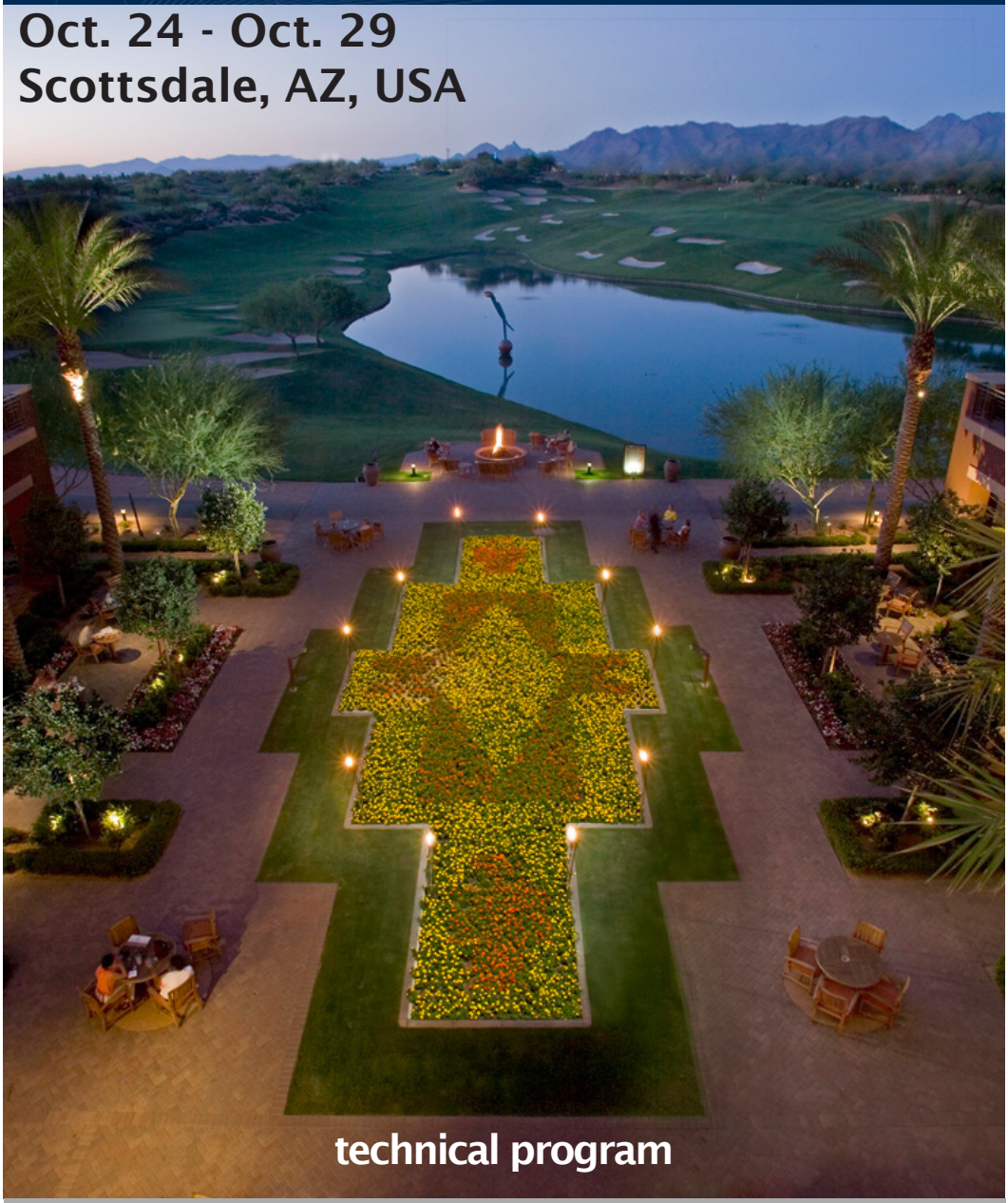
EMBEDDED SYSTEMS WEEK

Embedded Systems Week

www.esweek.org

Oct. 24 - Oct. 29
Scottsdale, AZ, USA



technical program

WELCOME TO SCOTTSDALE

On behalf of the Organizing Committee and the committees of our participating conferences - *CASES*, *CODES+ISSS*, and *EMSOFT* - we would like to welcome you Embedded Systems Week - *ESWEEK 2010* - in Scottsdale, Arizona. 2010 marks the 6th edition of *ESWEEK*. Earlier meetings were held in Jersey City, Seoul, Salzburg, Atlanta and Grenoble. This meeting has grown from two conferences and a handful of workshops to three conferences and a dynamic number of workshops that cover the most recent advances in embedded systems. *ESWEEK* is widely recognized as the premier technical event in embedded computing.

The combined program of the three conferences will offer three plenary keynotes and over 100 technical paper presentations. An industrial panel will conclude the conference. *ESWEEK* will also offer a number of half-day tutorials that survey hot topics of general interest to the embedded systems community. Additionally, the event will host eight workshops on a wide range of embedded systems topics that allow researchers and practitioners to share and discuss.

A complex event such as *ESWEEK* is a team effort that requires a dedicated group of volunteers to manage the success of the conference's growth in scale and offerings. We wish to thank every member of the organizing committee for their dedicated efforts in making the event a success. In particular, special thanks go to the following people for managing critical aspects of the conference organization: Franco Fummi for finances, Karam Chatha for local arrangements, Roman Lysecky for publications, Aviral Shrivastava for the conference website, Philipp Lucas for electronic media, Ahmed Jerraya and Karam Chatha for industrial contributions, Gabriela Nicolescu and Miguel Miranda for workshops and tutorials, and Wolfgang Rosenstiel for panels and special sessions. We also thank the Steering Committee members, the Program Chairs, and the Technical Program Committee members of each conference and workshop for selecting papers of the highest quality. ESWEEK continues to engage the active participation and involvement of industry. We greatly appreciate our major contributors: Intel, Xilinx, Cavium, Springer, the Artist Consortium and Arizona State University. Finally, we thank our sponsoring societies: ACM (SIGBED, SIGDA, SIGMICRO), IEEE (CAS, Computer, CEDA); and the cooperation with IFIP.

Scottsdale is situated in the greater Phoenix area which provides a perfect gateway to the natural beauty of the Grand Canyon state, Arizona. Besides the Heard museum (with one of finest collections of American Indian art), Frank Llyod Wright's Taliesin West, many championship quality golf courses, elegant resorts (including the conference site), the area also has a large number of microelectronics and embedded system companies. We therefore invite you to attend *ESWEEK 2010*, learn about the latest in embedded system technologies, and also discover the American Southwest.

HOTEL INFORMATION

The conference will be held at The Westin - Kierland Resort & Spa hotel, where all additional events will take place.

Special room rates are reserved for attendees.

	Sun 24	Mon 25	Tue 26	Wed 27	Thu 28	Fri 29
CASES	☐	■	■	■	☐	☐
CODES + ISSS	☐	■	■	■	☐	☐
EMSOFT	☐	■	■	■	☐	☐
Tutorials	■	☐	☐	☐	☐	☐
Workshops	■	☐	☐	☐	■	■
Page	8	9	10	11	12	13
SESSION LEGEND						A

Welcome Reception - Sunday, Oct. 24rd 2010 – 18:00 @ The Westin - Kierland Resort & Spa

Gala Banquet - Tuesday, Oct. 26th 2010 – 19:00 @ The Westin - Kierland Resort & Spa

Keynote: Monday Oct. 25, 2010

Embedded Market: Challenges and Opportunities

There is a convergence trend in the computing, communication and consumer markets and with a forecast of an additional 1 billion connected computing users by 2015, it is of high value to provide a common experience between the devices. Intel's vision of Compute Continuum will enable the users to realize the potential of a seamless cross-device experience with more consistency and accessibility to their information.

The convergence trend and the Compute Continuum make System-on-Chip [SoC] a key ingredient for the embedded markets. At Intel Labs, we are focusing on delivering differentiating technology solutions to enable our business partners to successfully capture their targeted market segments. We are working on a variety of research that will enable modular system architecture and silicon technology breakthroughs for rapid customization and integration facilitating faster time-to-market. Intel's vision along with some technology challenges and possible solutions will be highlighted.

Vida Ilderem,
Vice President, Intel Labs, Director, Integrated Platform Research Lab

Vida Ilderem is vice president of Intel Labs and director of the Integrated Platform Research Lab for Intel Corporation. The research lab focuses on deep integration on highly integrated platform-on-chip architectures as well as digital, analog and physical design factors.

Prior to joining Intel, Ilderem served as vice president of Systems and Technology Research at Motorola's Applied Research and Technology Center where she led research efforts that focused on delivering solutions for the next generation of communication and interaction technologies and integrated systems. She has also held the position of vice president of Physical & Digital Realization with focus on visual, computational and physical technologies, and served as director of RF/IF silicon technologies within Motorola's Semiconductor Products Sector.

Ilderem holds 27 issued patents and has been featured in numerous publications. She is a recipient of the Motorola's Distinguished Innovator Award.

Ilderem holds bachelor's degrees in electrical engineering and physics from Fresno State and a master's degree and doctorate degree in electrical engineering from the Massachusetts Institute of Technology (MIT).

Keynote: Tuesday Oct. 26, 2010

The Future of Computing from Phones to Warehouses: It's a New Day

John Hennessy,
President, Stanford University
John Hennessy received his B.E. in Electrical Engineering from Villanova University in 1973. He received his Masters and Ph.D. degrees in Computer Science from SUNY at Stony Brook in 1975 and 1977, respectively. Since September 1977, he has been a faculty member at Stanford University, where he is currently a Professor of Electrical Engineering and Computer Science.

Prior to becoming President, Professor Hennessy served as the University Provost, the Dean of the School of Engineering and was Chairman of the Computer Science Department.

Keynote: Wednesday Oct. 27, 2010

A Marketplace for Cloud Resources
Cloud computing is an emerging paradigm aimed to offer users pay-per-use computing resources, while leaving the burden of managing the computing infrastructure to the cloud provider.
We present a new programming and pricing model that gives the cloud user the flexibility of trading execution speed and price on a per-job basis. We discuss the scheduling and resource management challenges for the cloud provider that arise in the implementation of this model. We argue that techniques from real-time and embedded software can be useful in this context.

This is joint work with Anmol V. Singh, Vasu Singh, Thomas Wies, and Damien Zufferey.

Thomas A. Henzinger,
IST Austria
Tom Henzinger is President of IST Austria (Institute of Science and Technology Austria). He has a Ph.D. degree in Computer Science from Stanford University and held faculty positions at Cornell University, the University of California, Berkeley, the Max-Planck Institute for Computer Science, and EPFL. His research focuses on modern systems theory, especially models, algorithms, and tools for the design and analysis of software, hardware, and embedded systems. He is an ISI highly cited researcher, a member of Academia Europaea and of the German Academy of Sciences (Leopoldina), a Fellow of the ACM, and a dFellow of the IEEE.

	Room: Kierland 1A	Room: Kierland 1B	Room: Kierland 1C	Room: Powell A	Room: Cushing B	Room: Cushing A
8:00	TUTORIAL EMSOFT1 Model-based Analysis, Synthesis and Testing of Automotive Hardware/Software Architectures 8:00 – 12:00	TUTORIAL CASES1 MNEMEE – A Framework for Memory Management and Optimization of Static and Dynamic Data in MPSoC Systems 8:00 – 12:00	TUTORIAL CODES+ISSS1 Modeling and Analyzing Real-Time MultiProcessor Systems 8:00 – 12:00	WORKSHOP WFCD Artist Design Workshop on Foundations of Component Based Design 8:00 – 12:00	WORKSHOP WESS10 Workshop on Embedded Systems Security 8:00 – 12:00	WORKSHOP WCPS First Workshop in Diversity in Embedded Computing and Cyber-Physical Systems 8:00 – 12:00
9:00						
10:00						
11:00						
12:00						
13:00	TUTORIAL EMSOFT2 Quantitative System Validation in Model Driven Design 13:00 – 17:30	TUTORIAL CASES1 Challenges for Embedded Multicore Architectures 13:00 – 17:30	TUTORIAL CODES+ISSS2 Exploring Models of Computation using Ptolemy II 13:00 – 17:30	WORKSHOP WFCD Artist Design Workshop on Foundations of Component Based Design 13:00 – 17:30	WORKSHOP WESS10 Workshop on Embedded Systems Security 13:00 – 17:30	WORKSHOP WCPS First Workshop in Diversity in Embedded Computing and Cyber-Physical Systems 13:00 – 17:30
14:00						
15:00						
16:00						
17:00						
18:00	Welcome Reception @ The Westin – Kierland Resort and Spa 18:00					
19:00						

8:00

Opening Session
8:00 – 8:30

9:00

Keynote – Embedded Market: Challenges and Opportunities – Vida Ilderem
@ Kierland 2
8:30 – 9:30

Coffee break @ Hall of State
9:30 – 10:00

10:00

EMSOFT Session 1
@ Kierland 1C
10:00 – 12:00

CASES Session 1
@ Cushing
10:00 – 12:00

CODES+ISSS Session 1A
@ Kierland 1A
10:00 – 12:00

CODES+ISSS Session 1B
@ Kierland 1B
10:00 – 12:00

11:00

12:00

Lunch @ Pavillion
12:00 – 13:00

13:00

EMSOFT Session 2
@ Kierland 1C
13:00 – 15:00

CASES Session 2
@ Cushing
13:00 – 15:00

CODES+ISSS Session 2A
@ Kierland 1A
13:00 – 15:00

CODES+ISSS Session 2B
@ Kierland 1B
13:00 – 15:00

14:00

15:00

Coffee break @ Hall of State
15:00 – 15:30

16:00

EMSOFT Session 3
@ Kierland 1C
15:30 – 17:30

CASES Session 3
@ Cushing
15:30 – 17:30

CODES+ISSS Session 3A
@ Kierland 1A
15:30 – 17:30

CODES+ISSS Session 3B
@ Kierland 1B
15:30 – 17:30

17:00

18:00

SystemC User Group Meeting
@ Kierland 1A
18:00 – 21:00

19:00

OCT. 26

TUESDAY

10

ESWEEK 2010

8:00

9:00

10:00

EMSOFT Session 4
@ Kierland 1C
8:30 – 10:30

CASES Session 4
@ Cushing
8:30 – 10:30

CODES+ISSS Session 4A
@ Kierland 1A
8:30 – 10:30

CODES+ISSS Session 4B
@ Kierland 1B
8:30 – 10:30

Coffee break @ Hall of State
10:30 – 11:00

11:00

Keynote – John Hennessy
@ Kierland 2
11:00 – 12:00

12:00

Lunch @ Pavillion
12:00 – 13:00

13:00

EMSOFT Session 5
@ Kierland 1C
13:00 – 15:00

CASES Session 5
@ Cushing
13:00 – 15:00

CODES+ISSS Session 5A
@ Kierland 1A
13:00 – 15:00

CODES+ISSS Session 5B
@ Kierland 1B
13:00 – 15:00

14:00

15:00

Coffee break @ Hall of State
15:00 – 15:30

EMSOFT Session 6
@ Kierland 1C
15:30 – 17:30

CASES Session 6
@ Cushing
15:30 – 17:30

CODES+ISSS Session 6A
@ Kierland 1A
15:30 – 17:30

CODES+ISSS Session 6B
@ Kierland 1B
15:30 – 17:30

16:00

17:00

18:00

19:00

Gala Banquet
@ The Westin –Kierland Resort & Spa
19:00

8:00

9:00

Keynote – A Marketplace for Cloud Resources – Thomas A. Henzinger
@ Kierland 2
8:30 – 9:30

Coffee break @ Hall of State
9:30 – 10:00

10:00

11:00

EMSOFT Session 7
@ Kierland 1C
10:00 – 12:00

CASES Session 7
@ Cushing
10:00 – 12:00

CODES+ISSS Session 7A
@ Kierland 1A
10:00 – 12:00

CODES+ISSS Session 7B
@ Kierland 1B
10:00 – 12:00

12:00

Lunch @ Pavillion
12:00 – 13:00

13:00

14:00

EMSOFT Session 8
@ Kierland 1C
13:00 – 15:00

CASES Session 8
@ Cushing
13:00 – 15:00

CODES+ISSS Session 8A
@ Kierland 1A
13:00 – 15:00

CODES+ISSS Session 8B
@ Kierland 1B
13:00 – 15:00

15:00

Coffee break @ Hall of State
15:00 – 15:30

16:00

17:00

ESWEEK Industrial Panel
@ Kierland 2
15:30 – 17:30

18:00

19:00

	Room: Cushing A	Room: Powell A	Room: Powell B	Room: Lowell A
8:00	WORKSHOP ESTIMEDIA 8th IEEE Workshop on Embedded Systems for Real-Time Multimedia 8:00 – 12:00	WORKSHOP IWSSPS The Fifth International Workshop on Software Support for Portable Storage 8:00 – 12:00	WORKSHOP WESE Workshop on Embedded Systems Education 8:00 – 12:00	WORKSHOP CASA10 Workshop on Compiler Assisted SoC Assembly 8:00 – 12:00
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12:00	Lunch 12:00 – 13:00			
13:00	WORKSHOP ESTIMEDIA 8th IEEE Workshop on Embedded Systems for Real-Time Multimedia 13:00 – 17:30	WORKSHOP IWSSPS The Fifth International Workshop on Software Support for Portable Storage 13:00 – 17:30	WORKSHOP WESE Workshop on Embedded Systems Education 13:00 – 17:30	WORKSHOP CASA10 Workshop on Compiler Assisted SoC Assembly 13:00 – 17:30
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19:00				

	Room: Cushing A	Room: Cushing B
8:00	WORKSHOP ESTIMEDIA 8th IEEE Workshop on Embedded Systems for Real-Time Multimedia 8:00 – 12:00	WORKSHOP WSS'10 Workshop on Software Synthesis 8:00 – 12:00
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17:00		
18:00		
19:00		

October 25, Monday 10:00 - 12:00

EMSOFT

Room: Kierland 1C

Session 1: Verification & Synthesis
Session chair: Edward Lee

1.1 Automatic Verification of Control System Implementations.
Adolfo Anta, Rupak Majumdar, Indranil Saha and Paulo Tabuada

1.2 Switching Logic Synthesis for Reachability.
Ankur Taly and Ashish Tiwari

1.3 (S) Online Dynamic Stability Verification Using Sector Search.
Joseph Porter, Graham Hemingway, Chris vanBusKirk, Nicholas Kottenstette, Gabor Karsai and Janos Sztipanovits

1.4 (S) Components, Platforms and Possibilities: Towards Generic Automation for MDA.
Eunsuk Kang, Ethan Jackson, Dirk Seifert, Markus Dahlweid and Thomas Santen

CASES

Room: Cushing

Session 1: Compilers
Session chair: Scott Mahlke

1.1 Balancing Memory and Performance through Selective Flushing of Software Code Caches.
Apala Guha, Kim Hazelwood and Mary Lou Soffa

1.2 Erbium: A Deterministic, Concurrent Intermediate Representation to Map Data-Flow Tasks to Scalable, Persistent Streaming Processes.
Cupertino Miranda, Antoniu Pop, Philippe Dumont, Albert Cohen and Marc Duranton

1.3 Resource Recycling: Putting Idle Resources to Work on a Composable Accelerator.
Yongjun Park, Hyunchul Park, Scott Mahlke and Sukjin Kim

1.4 Instruction Selection by Graph Transformation.
Sebastian Buchwald and Andreas Zwinkau

CODES + ISSS

Room: Kierland 1A

Session 1A: Application-Specific Algorithms and Architectures
Session chair: Robert A. Walker
Session co-chair: Todor Stefanov

1.1 Rank Based Dynamic Voltage and Frequency Scaling for Tiled Graphics Processors (Best Paper Candidate).
B.V.N Silpa, Krishnaiah Gummidipudi and Preeti Ranjan Panda

1.2 Immediate Fabrics: Virtual Architectures for Circuit Portability and Fast Placement and Routing.
James Coole and Greg Stitt

1.3 An Elastic Software Cache with Fast Prefetching for Motion Compression in Video Decoding.
Ping Chao and Youn-Long Lin

Room: Kierland 1B

Session 1B: Reconfigurable and Real-time Systems
Session chair: Sudarshan Banerjee
Session co-chair: Pai Chou

1.1 Verification of Dynamically Reconfigurable Embedded systems by Model Transformation Rules.
Felix Madlener, Julia Weingart and Sorin A. Huss

1.2 Hardware/Software Optimization of Error Detection Implementation for Real-time Embedded Systems.
Adrian Lifa, Petru Eles, Zebo Peng and Viacheslav Izosimov

1.3 Scheduling Garbage Collection in Realtime Systems.
Martin Kero and Simon Aittamaa

POSTER SESSION @ 11:30

POSTER SESSION @ 11:30

October 25, Monday 13:00 - 15:00

EMSOFT

Room: Kierland 1C

Session 2: Applications and Tools
Session chair: Rodric Rabbah

2.1 Parallelizing the H.264 Decoder on the Cell BE Processor.
Yongjin Cho, Seungkyun Kim, Jaejin Lee and Heonshik Shin

2.2 Optimal WCET-Aware Code Selection for Scratchpad Memory.
Hui Wu, Jingling Xue and Sri Parameswaran

2.3 (S) A Model Based Approach for Debugging Embedded Systems in Real Time.
Padma Iyenghar, Clemens Westerkamp, Juergen Wuebbelmann and Elke Pulvermueller

2.4 (S) PinaVM: a SystemC Front-End Based on an Executable Intermediate Representation.
Kevin Marquet and Matthieu Moy

CASES

Room: Cushing

Session 2: Special session -- Embedded Systems for Future Medical Care
Session chair: Vincent J. Mooney

2.1 Routing-Based Synthesis of Digital Microfluidic Biochips.
Elena Maftei, Paul Pop and Jan Madsen

2.2 Mosaic of Organic Development Through Technology Intervention in the Rural Indian Context.
Pingali Rajeswarii and P. Niranjana
(invited)

2.3 The Virtual Hospital.
Danny Petrasek, M.D.
(invited)

2.4 Parsimonious Information Technologies for Pixels, Perception, Wetware and Simulation
Alan Barr
(invited)

CODES + ISSS

Room: Kierland 1A

Session 2A: Special Session - From ESL-2010 to ESL-2015
Session chairs: Adam Donlin (Xilinx) and Karam Chatha (Arizona State University)

ESL and Modeling: Time to Get Rid of the Duct Tape and Bailing Wire.
Tor Jeremiassen, Texas Instruments.

Putting Virtual Prototypes Into Action,
Tim Koegel, Synopsys.

ESL Analysis, Verification and Synthesis of SoCs,
Andres Takach, Mentor Graphics

ESL 2015: The inevitable move to software programmability.
Grant Martin, Tensilica.

Room: Kierland 1B

Session 2B: Special Session - HW/SW Co-design for High Performance Computing: challenges and opportunities
Session chairs: X. Sharon Hu (Notre Dame) and Richard Murphy (Sandia)

A new era of HPC System Design.
Sudip Dosanjh, Sandia National Labs

Who were the enemies of high-performance computing system design in the pass 20+ years?
Stephen Poole, US DoE/DoD

HW/SW Specialization for Heterogeneous Parallelism.
Kunle Olukotun, Stanford University

Research/funding opportunities in codesign for HPC systems.
Bill Harrod, DARPA

POSTER SESSION @ 14:30

October 25, Monday 15:30 - 17:30

EMSOFT

Room: Kierland 1C

Session 3: Scheduling & Optimization
Session chair: Alessandro Pinto

3.1 Online Robust Optimization Framework for QoS Guarantees in Distributed Soft Real-Time Systems.
Jinkyu Lee, Insik Shin and Arvind Easwaran

3.2 Load-Based Schedulability Analysis of Certifiable Mixed-Criticality Systems.
Haohan Li and Sanjoy Baruah

3.3 Reducing Stack with Intra-Task Threshold Priorities in Real-Time Systems.
Gang Yao and Giorgio Buttazzo

POSTER SESSION @ 17:00

CASES

Room: Cushing

Session 3: Architectures
Session chair: Aviral Shrivastava

3.1 Implementing Virtual Secure Circuit Using A Custom-Instruction Approach.
Zhimin Chen, Ambuj Sinha and Patrick Schaumont

3.2 Mighty-Morphing Power-SIMD.
Ganesh Dasika, Mark Woh, Sangwon Seo, Trevor Mudge, Nathan Clark and Scott Mahlke

3.3 Towards Minimizing Reconfiguration Overhead in Dynamically Reconfigurable Processors: REDEFINE as a case study.
Ratna Krishnamoorthy, Keshavan Varadarajan, Ganesh Garga, Mythri Alle, Ranjani Narayan, Masahiro Fujita and S. K. Nandy

POSTER SESSION @ 17:00
MEET TODAY'S AUTHORS

CODES + ISSS

Room: Kierland 1A

Session 3A: Optimising Multiprocessor and NoC Platforms for Performance, QoS, and Reliability
Session chair: Rainer Dömer
Session co-chair: Frank Vahid

3.1 Exploring Programming Model-driven QoS Support for NoC-based Platforms (Best Paper Candidate).
Jaume Joven, Andrea Marongiu, Federico Angiolini and Luca Benini

3.2 Optimal Synthesis of Latency and Throughput Constrained Pipelined MPSoCs targeting Streaming Applications.
Haris Javaid, Xin He, Aleksander Ignjatovic and Sri Parameswaran

3.3 OE+IOE: A Novel Turn Model Based Fault Tolerant Routing Scheme for Network-on-Chip.
Sudeep Pasricha, Yong Zou, Dan Connors and HJ Siegel

Room: Kierland 1B

Session 3B: Power-Aware Design
Session chair: Sarma Vrudhula
Session co-chair: Naehyuck Chang

3.1 Power Aware SID-based Simulator for Embedded Multicore DSP Subsystems.
Cheng-Yen Lin, Po-Yu Chen, Chun-Kai Tseng, Chung-Wen Huang, Chia-Chieh Weng, Chi-Bang Kuan, Shih-Han Lin, Shi-Yu Huang and Jenq-Kuen Lee

3.2 Accurate Online Power Estimation and Automatic Battery Behavior Based Power Model Generation for Smartphones.
Lide Zhang, Birjodh Tiwana, Zhiyun Qian, Zhaoguan Wang, Robert Dick, Morley Mao and Lei Yang

3.3 Statistical Approach in a System Level Methodology to Deal With Process Variation.
Concepción Sanz, Manuel Prieto, José Ignacio Gómez, Christian Tenllado and Francky Catthoor

POSTER SESSION @ 17:00

October 26, Tuesday 8:30 - 10:30

EMSOFT

Room: Kierland 1C

Session 4: Automotive & Wireless Sensor Networks
Session chair: Ken Butts

4.1 Modeling Buffers with Data Refresh Semantics in Automotive Architectures.
Linh Thi Xuan Phan, Reinhard Schneider, Samarjit Chakraborty and Insup Lee

4.2 Schedulability and End-to-end Latency in Distributed ECU Networks: Formal Modeling and Precise Estimation.
A. C. Rajeev, Swarup Mohalik, Manoj G. Dixit, Devesh B. Chokshi and S. Ramesh

4.3 (S) TeleScribe: A Scalable, Resumable Wireless Reprogramming Approach.
Min-Hua Chen and Pai Chou

4.4 (S) Nucleos: a Runtime System for Ultra-Compact Wireless Sensor Nodes.
Jiwon Hahn and Pai Chou

POSTER SESSION @ 10:00

CASES

Room: Cushing

Session 4: Architectures
Session chair: Lothar Thiele

4.1 Implementing Dynamic Implied Addressing Mode for Multi-Output Instructions.
Jonghee M. Youn, Jongwon Lee, Yunheung Paek, Jongwung Kim and Jeonghun Cho

4.2 Real-time Unobtrusive Program Execution Trace Compression Using Branch Predictor Events.
Vladimir Uzelac, Aleksandar Milenkovic, Martin Burtscher and Milena Milenkovic

4.3 A Memory Interface for Multi-Purpose Multi-Stream Accelerators.
Sylvain Girbal, Olivier Temam, Sami Yehia, Hugues Berry and Zheng Li

4.4 Hardware-Based Data Value and Address Trace Filtering Techniques.
Vladimir Uzelac and Aleksandar Milenkovic

CODES + ISSS

Room: Kierland 1A

Session 4A: MPSoC: Analysis and Synthesis
Session chair: Andreas Gerstlauer
Session co-chair: Roman Lysecky

4.1 Worst-case Performance Analysis of Synchronous Dataflow Scenarios (Best Paper Candidate).
Marc Geilen

4.2 Improving Platform-Based System Synthesis by Satisfiability Modulo Theories Solving.
Felix Reimann, Michael Glass, Christian Haubelt, Michael Eberl and Jürgen Teich

4.3 A Case for Lifetime-Aware Task Mapping in Embedded Chip Multiprocessors.
Adam Hartman, Donald Thomas and Brett Meyer

Room: Kierland 1B

Session 4B: Memory and Communication Architecture
Session chair: Sundeep Pasricha
Session co-chair: Christian Haubelt

4.1 Automatic Memory Partitioning: Increasing Memory Parallelism via Data Structure Partitioning.
Nadav Rotem and Yosi Ben Asher

4.2 Towards a Synthesis Semantics for SystemC Channels.
Kim Grüttner, Henning Kleen, Frank Oppenheimer, Achim Rettberg and Wolfgang Nebel

4.3 Demand-based Block-level Address Mapping in Large-scale NAND Flash Storage Systems.
Zhiwei Qin, Yi Wang, Duo Liu and Zili Shao

POSTER SESSION @ 10:00

October 26, Tuesday 13:00 - 15:00

EMSOFT

Room: Kierland 1C

Session 5: Flash Memory
Session chair: Dimitrios Soudris

5.1 Using NAND Flash Memory for Executing Large Volume Real-Time Programs in Automotive Embedded Systems.
Kwangyoon Cho, Kyoung-Soo We, Chang-Gun Lee and Kanghee Kim

5.2 Janus-FTL: Finding Optimal Point on the Spectrum between Page and Block Mapping Schemes.
Hunki Kwon, Eunsam Kim, Jongmoo Choi, Donghee Lee and Sam H. Noh

5.3 A Reliable MTD Design for MLC Flash-Memory Storage Systems.
Yuan-Hao Chang and Tei-Wei Kuo

CASES

Room: Cushing

Session 5: Compiler Managed Caches/Memories
Session chair: Rodric Rabbah

5.1 Improving Scratchpad Allocation with Demand-Driven Data Tiling.
Li Wang, Xuejun Yang, Jingling Xue, Tao Tang, Xiaoguang Ren and Shen Ye

5.2 Fine-grain Dynamic Instruction Placement for L0 Scratch-pad Memory.
Jongsoo Park, James Balfour and William Dally

5.3 Improved Procedure Placement for Set Associative Caches.
Yun Liang and Tulika Mitra

5.4 Minimizing Inter-Task Interferences in Scratch-Pad Memory Usage for Reducing the Energy Consumption of Multi-Task Systems.
Lovic Gauthier, Tohru Ishihara, Hideki Takase, Hiroyuki Tomiyama and Hiroaki Takada

CODES + ISSS

Room: Kierland 1A

Session 5A: Embedded Tutorial - An Introduction to the SystemC Synthesis Subset Standard
Session Chairs:

Introduction to high-level synthesis & SystemC synthesis subset.
Philippe Coussy, Université de Bretagne-Sud

Achieving high-quality hardware results using SystemC synthesis.
Mike Meredith, Forte Design Systems

Synthesizing systems containing both algorithmic and control blocks from high-level SystemC specifications using HLS.
Andres Takach, Mentor Graphics

SystemC synthesizability at the pin and transaction levels.
Mike McNamara, Cadence

Room: Kierland 1B

Session 5B: Embedded Tutorial - Compilation techniques for CGRAs: Exploring all parallelization approaches
Session chair: Tom Vander Aa (IMEC)

Polymorphic pipeline arrays, expanding coarse-grained arrays beyond innermost loops.
Scott Mahlke, University of Michigan

Code-generation for coarse-grained arrays: flexibility and programmer productivity.
Bjorn De Sutter, Ghent University

Memory-aware compilation techniques for CGRAs.
Aviral Shrivastava, Arizona State University

Retargetable Mapping of Loop Programs on Coarse-grained Reconfigurable Arrays.
Frank Hannig, Erlangen University

POSTER SESSION @ 14:30

October 26, Tuesday 15:30 - 17:30

EMSOFT

Room: Kierland 1C

Session 6: Distribution & Event Graphs
Session chair: Walid Taha

6.1 A Unifying View of Loosely Time-Triggered Architectures.
Albert Benveniste, Anne Bouillard and Paul Caspi

6.2 Semantics-Preserving Implementation of Synchronous Specifications over Dynamic TDMA Distributed Architectures.
Dumitru Potop-Butucaru, Akramul Azim and Sebastian Fischmeister

6.3 (S) From High-level Component-Based Models to Distributed Implementations.
Borzoo Bonakdarpour, Marius Bozga, Mohamad Jaber, Jean Quilbeuf and Joseph Sifakis

6.4 (S) Ptera: An Event-Oriented Model of Computation for Heterogeneous Systems.
Thomas Huining Feng, Edward A. Lee and Lee W. Schruben

CASES

Room: Cushing

Session 6: Special Session: IEEE McDowell Lecture and Novel Architectures
Session chair: Vinod Kathail/Reid Tatge

6.1 Compilers, Architectures and Synthesis for Embedded Computing: Retrospect and Prospect.
Prof. Krishna Palem

6.2 Optimizing Energy to Minimize Errors in Dataflow Graphs Using Approximate Adders.
Zvi Kedem, Vincent Mooney, Kirthi Krishna, Krishna Palem, Avani Devarasetty and Phanideepak Parasuramuni

CODES + ISSS

Room: Kierland 1A

Session 6A: Memory architecture for embedded systems
Session chair: Joerg Henkel
Session co-chair: Andy Pimentel

6.1 Dynamic, Non-Linear Cache Architecture for Power-Sensitive Mobile Processors.
Garo Bournoutian and Alex Orailoglu

6.2 A Greedy Buffer Allocation Algorithm for Power-aware Communication in Body Sensor Networks.
Hassan Ghasemzadeh and Roozbeh Jafari

6.3 High Durability in NAND Flash Memory through Effective Page Reuse Mechanisms.
Kwangyoon Lee and Alex Orailoglu

Room: Kierland 1B

Session 6B: New Design Approaches for Network-on-Chip Systems
Session chair: Sundeep Pasricha
Session co-chair: Kees Goossens

6.1 A Holistic Approach to Network-on-Chip Synthesis.
Glenn Leary and Karam Chatha

6.2 NeuroNoC: Neural Network Inspired Runtime Adaptation for an On-chip Communication Architecture.
Thomas Ebi, Mohammad Abdullah Al Faruque and Jörg Henkel

6.3 Workload Characterization and its Impact on Multicore Platform Design.
Paul Bogdan and Radu Marculescu

6.4 Mini panel.
Moderator: Petru Eles

POSTER SESSION @ 17:00

October 27, Wednesday 10:00 - 12:00

EMSOFT

Room: Kierland 1C

Session 7: Model-Based Design & Patterns
Session chair: Lothar Thiele

7.1 Model-Based Implementation of Real-Time Applications.
Tesnim Abdellatif, Jacques Combaz and Joseph Sifakis

7.2 Model-based Specification of Timing Requirements.
Christian Buckl, Irina Gaponova, Michael Geisinger, Alois Knoll and Edward Lee

7.3 Initiating a Design Pattern Catalog for Embedded Network Systems.
Sally K. Wahba, Jason O. Hallstrom and Neelam Soundarajan

CASES

Room: Cushing

Session 7: Compilers
Session chair: Tulika Mitra

7.1 Eliminating False Phase Interactions to Reduce Optimization Phase Order Search Space.
Michael Jantz and Prasad Kulkarni

7.2 Practical Aggregation of Semantical Program Properties for Machine Learning Based Compilation.
Mircea Namolaru, Albert Cohen, Grigori Fursin, Ayal Zaks and Ari Freund

7.3 Vertical Stealing: Robust, Locality-Aware Do-All Workload Distribution for 3D MPSoCs.
Andrea Marongiu, Paolo Burgio and Luca Benini

7.4 Design space exploration of the Turbo decoding algorithm on the NVIDIA GPU
Dongwon Lee, Marilyn Wolf and Hyesoon Kim

CODES + ISSS

Room: Kierland 1A

Session 7A: Novel techniques for accelerating system simulation
Session chair:
Session co-chair:

7.1 parSC: Synchronous Parallel SystemC Simulation on Multi-Core Host Architectures.
Christoph Schumacher, Rainer Leupers, Dietmar Petras and Andreas Hoffmann

7.2 FastFwd: An Efficient Hardware Acceleration Technique for Trace-driven Network-on-Chip Simulation.
Krishnaiah Gummidipudi, B.V.N Silpa, Preeti Ranjan Panda and Anshul Kumar

7.3 FEMU: A Firmware-Based Emulation Framework for SoC Verification.
Hao Li, Dong Tong, Kan Huang and Xu Cheng

Room: Kierland 1B

Session 7.B: Embedded Software Performance Optimization
Session chair: Aviral Shrivastava
Session co-chair: Preeti Ranjan Panda

7.1 Automatic Parallelization of Embedded Software Using Hierarchical Task Graphs and Integer Linear Programming.
Daniel Cordes, Peter Marwedel and Arindam Mallik

7.2 Performance Modeling of Embedded Applications with Zero Architectural Knowledge.
Marco Lattuada and Fabrizio Ferrandi

7.3 A Performance Model and Code Overlay Generator for Scratchpad Enhanced Embedded Processors.
Michael Baker, Amrit Panda, Nikhil Ghadge, Aniruddha Kadne and Karam Chatha

POSTER SESSION @ 11:30

October 27, Wednesday 13:00 - 15:00

EMSOFT

Room: Kierland 1C

Session 8: Scheduling & Control
Session chair: Nicolas Halbwachs

8.1 Power-Aware Temporal Isolation with Variable-Bandwidth Servers.Silviu Craciunas, Christoph Kirsch and Ana Sokolova

8.2 Resource Adaptations with Servers for Hard Real-Time Systems.
Nikolay Stoimenov, Lothar Thiele, Luca Santinelli and Giorgio Buttazzo

8.3 (S) Energy-Aware Packet and Task Co-Scheduling for Embedded Systems.
Luca Santinelli, Mauro Marinoni, Francesco Prosperi, Francesco Esposito, Gianluca Franchino and Giorgio Buttazzo

8.4 (S) Dynamic Tuning of Feature Set in Highly Variant Interactive Applications.
Tushar Kumar, Romain Cledat and Santosh Pande

CASES

Room: Cushing

Session 8: Cache and Memory Architectures
Session chair: Oliver Bringmann

8.1 Characterization and Exploitation of Narrow-Width Loads: The Narrow-Width Cache Approach.
Mafijul Md Islam and Per Stenstrom

8.2 E < MC^2 : Less Energy through Multi-Copy Cache.
Arup Chakraborty, Houman Homayoun, Amin Khajeh, Nikil Dutt, Ahmed Eltawil and Fadi Kurdahi

8.3 Enabling Large Decoded Instruction Loop Caching for Energy-Aware Embedded Processors.
Ji Gu and Hui Guo

CODES + ISSS

Room: Kierland 1A

Session 8A: Reliability and Memory Issues in MPSoCs
Session chair: Aseem Gupta
Session co-chair: Paul Pop

8.1 System-Level Reliability Modeling of MPSoCs.
Yun Xiang, Thidapat Chantem, Robert Dick, Sharon Hu and Li Shang

8.2 A Task Re-Mapping Technique for Reliable Multi-core Embedded Systems.
Chanhee Lee, Hokeun Kim, Hae-woo Park, Sungchan Kim, Hyunok Oh and Soonhoi Ha

8.3 Heap Data Management for Limited Local Memory (LLM) Multi-core Processors.
Ke Bai and Aviral Shrivastava

Room: Kierland 1B

Session 8B: Special Session - Unconventional Fabrics, Architectures, and Models for Future Multi-core Systems
Session chair: Radu Marculescu

Self-assembled Nanoscale On-Chip Interconnect: The Good, the Bad and the Ugly.
Christof Teuscher, Portland State University

Small-World Hybrid Wireless Network-on-Chip Architecture for Massive Multi-Core Systems.
Partha Pande, Washington State University

Is the Network the Real Problem for Future Multi-core Systems?
Radu Marculescu, CMU

POSTER SESSION @ 14:30

ESWEEK Industrial PANEL

Wednesday, Oct. 27th 2010
15:30

The future of embedded architectures

Organizers: Wolfgang Rosenstiel, Karamvir S. Chatha

Moderator: Alberto L Sangiovanni-Vincentelli

Panelists:

~ Pranav Mehta
Senior Principal Engineer and Chief Technology Officer of Intel's Embedded and Communications Group

~ Nat Seshan
Distinguished Member Technical Staff, Director of DSP Architecture, Texas Instruments

~ Grant Martin
Chief Scientist, Tensilica Inc.

~ Jim Holt
Manager, Processor Core Architecture and Modeling, Networking and Multimedia Group, Freescale Inc.

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