On behalf of the Organizing Committee and the committees of our participating conferences - CASES, CODES+ISSS, and EMSOFT - we would like to welcome you Embedded Systems Week - ESWEEK 2010 - in Scottsdale, Arizona. 2010 marks the 6th edition of ESWEEK. Earlier meetings were held in Jersey City, Seoul, Salzburg, Atlanta and Grenoble. This meeting has grown from two conferences and a handful of workshops to three conferences and a dynamic number of workshops that cover the most recent advances in embedded systems. ESWEEK is widely recognized as the premier technical event in embedded computing.

The combined program of the three conferences will offer three plenary keynotes and over 100 technical paper presentations. An industrial panel will conclude the conference. ESWEEK will also offer a number of half-day tutorials that survey hot topics of general interest to the embedded systems community. Additionally, the event will host eight workshops on a wide range of embedded systems topics that allow researchers and practitioners to share and discuss.

A complex event such as ESWEEK is a team effort that requires a dedicated group of volunteers to manage the success of the conference’s growth in scale and offerings. We wish to thank every member of the organizing committee for their dedicated efforts in making the event a success. In particular, special thanks go to the following people for managing critical aspects of the conference organization: Franco Fummi for finances, Karam Chatha for local arrangements, Roman Lysecky for publications, Aviral Shrivastava for the conference website, Philipp Lucas for electronic media, Ahmed Jerraya and Karam Chatha for industrial contributions, Gabriela Nicolescu and Miguel Miranda for workshops and tutorials, and Wolfgang Rosenstiel for panels and special sessions. We also thank the Steering Committee members, the Program Chairs, and the Technical Program Committee members of each conference and workshop for selecting papers of the highest quality. ESWEEK continues to engage the active participation and involvement of industry. We greatly appreciate our major contributors: Intel, Xilinx, Cavium, Springer, the Artist Consortium and Arizona State University. Finally, we thank our sponsoring societies: ACM (SIGBED, SIGDA, SIGMICRO), IEEE (CAS, Computer, CEDA); and the cooperation with IFIP.

Scottsdale is situated in the greater Phoenix area which provides a perfect gateway to the natural beauty of the Grand Canyon state, Arizona. Besides the Heard museum (with one of finest collections of American Indian art), Frank Llyod Wright’s Taliesin West, many championship quality golf courses, elegant resorts (including the conference site), the area also has a large number of microelectronics and embedded system companies. We therefore invite you to attend ESWEEK 2010, learn about the latest in embedded system technologies, and also discover the American Southwest.
HOTEL INFORMATION

The conference will be held at The Westin - Kierland Resort & Spa hotel, where all additional events will take place.

Special room rates are reserved for attendees.
Welcome Reception - Sunday, Oct. 24\textsuperscript{rd} 2010 – 18:00
@ The Westin - Kierland Resort & Spa

Gala Banquet - Tuesday, Oct. 26\textsuperscript{th} 2010 – 19:00
@ The Westin - Kierland Resort & Spa
Embedded Market: Challenges and Opportunities
There is a convergence trend in the computing, communication and consumer markets and with a forecast of an additional 1 billion connected computing users by 2015, it is of high value to provide a common experience between the devices. Intel’s vision of Compute Continuum will enable the users to realize the potential of a seamless cross-device experience with more consistency and accessibility to their information.
The convergence trend and the Compute Continuum make System-on-Chip [SoC] a key ingredient for the embedded markets. At Intel Labs, we are focusing on delivering differentiating technology solutions to enable our business partners to successfully capture their targeted market segments. We are working on a variety of research that will enable modular system architecture and silicon technology breakthroughs for rapid customization and integration facilitating faster time-to-market. Intel’s vision along with some technology challenges and possible solutions will be highlighted.

Vida Ilderem,
Vice President, Intel Labs, Director, Integrated Platform Research Lab
Vida Ilderem is vice president of Intel Labs and director of the Integrated Platform Research Lab for Intel Corporation. The research lab focuses on deep integration on highly integrated platform-on-chip architectures as well as digital, analog and physical design factors.
Prior to joining Intel, Ilderem served as vice president of Systems and Technology Research at Motorola’s Applied Research and Technology Center where she led research efforts that focused on delivering solutions for the next generation of communication and interaction technologies and integrated systems. She has also held the position of vice president of Physical & Digital Realization with focus on visual, computational and physical technologies, and served as director of RF/IF silicon technologies within Motorola’s Semiconductor Products Sector.
Ilderem holds 27 issued patents and has been featured in numerous publications. She is a recipient of the Motorola’s Distinguished Innovator Award.
Ilderem holds bachelor’s degrees in electrical engineering and physics from Fresno State and a master’s degree and doctorate degree in electrical engineering from the Massachusetts Institute of Technology (MIT).
Keynote: Tuesday Oct. 26, 2010

The Future of Computing from Phones to Warehouses: It’s a New Day

John Hennessy,
President, Stanford University
John Hennessy received his B.E. in Electrical Engineering from Villanova University in 1973. He received his Masters and Ph.D. degrees in Computer Science from SUNY at Stony Brook in 1975 and 1977, respectively. Since September 1977, he has been a faculty member at Stanford University, where he is currently a Professor of Electrical Engineering and Computer Science.

Prior to becoming President, Professor Hennessy served as the University Provost, the Dean of the School of Engineering and was Chairman of the Computer Science Department.
Keynote: Wednesday Oct. 27, 2010

A Marketplace for Cloud Resources
Cloud computing is an emerging paradigm aimed to offer users pay-per-use computing resources, while leaving the burden of managing the computing infrastructure to the cloud provider.
We present a new programming and pricing model that gives the cloud user the flexibility of trading execution speed and price on a per-job basis. We discuss the scheduling and resource management challenges for the cloud provider that arise in the implementation of this model. We argue that techniques from real-time and embedded software can be useful in this context.

This is joint work with Anmol V. Singh, Vasu Singh, Thomas Wies, and Damien Zufferey.

Thomas A. Henzinger,
IST Austria
Tom Henzinger is President of IST Austria (Institute of Science and Technology Austria). He has a Ph.D. degree in Computer Science from Stanford University and held faculty positions at Cornell University, the University of California, Berkeley, the Max-Planck Institute for Computer Science, and EPFL. His research focuses on modern systems theory, especially models, algorithms, and tools for the design and analysis of software, hardware, and embedded systems. He is an ISI highly cited researcher, a member of Academia Europaea and of the German Academy of Sciences (Leopoldina), a Fellow of the ACM, and a dFellow of the IEEE.
## Tutorial Schedule

<table>
<thead>
<tr>
<th>Time</th>
<th>Session Name</th>
<th>Location</th>
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<tbody>
<tr>
<td>8:00 - 12:00</td>
<td>TUTORIAL CASES1</td>
<td>Room: Kierland 1A</td>
</tr>
<tr>
<td></td>
<td>MNEMEE - A Framework for Memory Management and Optimization of Static and Dynamic Data in MPSoC Systems</td>
<td>Room: Kierland 1B</td>
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<tr>
<td>8:00 - 12:00</td>
<td>TUTORIAL EMSSOF1</td>
<td>Room: Powell A</td>
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<tr>
<td></td>
<td>Model-based Analysis, Synthesis and Testing of Automotive Hardware/Software Architectures</td>
<td>Room: Cushing B</td>
</tr>
<tr>
<td>8:00 - 12:00</td>
<td>TUTORIAL CODES+ISSS1</td>
<td>Room: Cushing A</td>
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<tr>
<td></td>
<td>Modeling and Analyzing Real-Time MultiProcessor Systems</td>
<td>Room: Kierland IC</td>
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<tr>
<td>13:00 - 17:30</td>
<td>TUTORIAL CASES1</td>
<td>Room: Kierland 1A</td>
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<tr>
<td></td>
<td>Challenges for Embedded Multicore</td>
<td>Room: Kierland 1B</td>
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<tr>
<td>13:00 - 17:30</td>
<td>TUTORIAL EMSSOF2</td>
<td>Room: Cushing B</td>
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<tr>
<td></td>
<td>Quantitative System Validation in Model Driven Design</td>
<td>Room: Cushing A</td>
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<tr>
<td>13:00 - 17:30</td>
<td>TUTORIAL CODES+ISSS2</td>
<td>Room: Cushing A</td>
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<td></td>
<td>Exploring Models of Computation using Ptolemy II</td>
<td>Room: Kierland IC</td>
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## Workshop Schedule

<table>
<thead>
<tr>
<th>Time</th>
<th>Session Name</th>
<th>Location</th>
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<tbody>
<tr>
<td>8:00 - 12:00</td>
<td>WORKSHOP WFCD</td>
<td>Room: Kierland 1A</td>
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<td>Artist Design Workshop on Foundations of Embedded Systems in MultiCore Systems</td>
<td>Room: Kierland 1B</td>
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<tr>
<td>8:00 - 12:00</td>
<td>WORKSHOP WESS10</td>
<td>Room: Powell A</td>
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<td></td>
<td>Workshop on Embedded Systems</td>
<td>Room: Cushing B</td>
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<tr>
<td>8:00 - 12:00</td>
<td>WORKSHOP WCPS</td>
<td>Room: Cushing A</td>
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<td>First Workshop in Cyber-Physical Computing and Embedded Diversity in First Workshop in</td>
<td>Room: Kierland IC</td>
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<tr>
<td>13:00 - 17:30</td>
<td>WORKSHOP WESS10</td>
<td>Room: Kierland 1A</td>
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## Welcome Reception

Welcome Reception @ The Westin - Kierland Resort and Spa

18:00
<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
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<tbody>
<tr>
<td>8:00</td>
<td>Opening Session</td>
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<td>8:00 - 8:30</td>
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<tr>
<td>9:00</td>
<td>Keynote - Embedded Market: Challenges and Opportunities – Vida Ilderem</td>
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<td></td>
<td>@ Kierland 2</td>
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<tr>
<td></td>
<td>8:30 – 9:30</td>
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<tr>
<td>10:00</td>
<td>Coffee break @ Hall of State</td>
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<td>9:30 – 10:00</td>
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<td>11:00</td>
<td>EMSOFT Session 1</td>
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<td>@ Kierland 1C</td>
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<td>10:00 – 12:00</td>
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<td>12:00</td>
<td>Lunch @ Pavilion</td>
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<td>12:00 – 13:00</td>
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<td>13:00</td>
<td>EMSOFT Session 2</td>
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<tr>
<td></td>
<td>@ Kierland 1C</td>
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<td></td>
<td>13:00 – 15:00</td>
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<tr>
<td>14:00</td>
<td>Coffee break @ Hall of State</td>
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<td>15:00 – 15:30</td>
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<td>15:00</td>
<td>EMSOFT Session 3</td>
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<td>@ Kierland 1C</td>
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<td>15:30 – 17:30</td>
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<tr>
<td>16:00</td>
<td>SystemC User Group Meeting</td>
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<tr>
<td></td>
<td>@ Kierland 1A</td>
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<td>18:00 – 21:00</td>
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</table>
19:00 Gala Banquet @ The Westin – Kierland Resort & Spa

08:00 Coffee break @ Hall of State

08:30 - 10:30 CODES+ISSS Session 4B @ Kierland 1B
08:30 - 10:30 CODES+ISSS Session 6A @ Kierland 1A
08:30 - 10:30 CODES+ISSS Session 4A @ Kierland 1A
10:30 - 11:00 Keynote – John Hennessy @ Kierland 2

10:30 - 12:00 CODES+ISSS Session 5A @ Kierland 1A
10:30 - 12:00 CASES Session 5 @ Cushing
10:30 - 12:00 CODES+ISSS Session 5B @ Kierland 1B
10:30 - 12:00 EMOSFT Session 5 @ Kierland 1C
12:00 - 13:00 Lunch @ Pavillion

13:00 - 15:00 CODES+ISSS Session 6A @ Kierland 1A
13:00 - 15:00 CASES Session 6 @ Cushing
13:00 - 15:00 CODES+ISSS Session 6B @ Kierland 1B
13:00 - 15:00 EMOSFT Session 6 @ Kierland 1C
15:00 - 15:30 Coffee break @ Hall of State

16:00 - 17:30 CODES+ISSS Session 7A @ Kierland 1A
16:00 - 17:30 CASES Session 7 @ Cushing
16:00 - 17:30 CODES+ISSS Session 7B @ Kierland 1B
16:00 - 17:30 EMOSFT Session 7 @ Kierland 1C
17:30 - 18:00 Coffee break @ Hall of State

18:00 - 20:00 Gala Banquet @ The Westin – Kierland Resort & Spa
Room: Cushing A

WORKSHOP
ESTIMEDIA
8th IEEE Workshop on Embedded Systems for Real-Time Multimedia
8:00 - 12:00

Room: Cushing B

WORKSHOP
WSS’10
Workshop on Software Synthesis
8:00 - 12:00
Session 1: Compilers
Session chair: Scott Mahlke
1.1 Balancing Memory and Performance through Selective Flushing of Software Code Caches.
   Apala Guha, Kim Hazelwood and Mary Lou Soffa
1.2 Erbium: A Deterministic, Concurrent Intermediate Representation to Map Data-Flow Tasks to Scalable, Persistent Streaming Processes.
   Cupertino Miranda, Antoniu Pop, Philippe Dumont, Albert Cohen and Marc Duranton
1.3 Resource Recycling: Putting Idle Resources to Work on a Composable Accelerator.
   Yongjun Park, Hyunchul Park, Scott Mahlke and Sukjin Kim
1.4 Instruction Selection by Graph Transformation.
   Sebastian Buchwald and Andreas Zwickau

Session 1A: Application-Specific Algorithms and Architectures
Session chair: Robert A. Walker
Session co-chair: Todor Stefanov
1.1 Rank Based Dynamic Voltage and Frequency Scaling for Tiled Graphs (Best Paper Candidate).
   B.V.N Silpa, Krishnaiah Gummidipudi and Preeti Ranjan Panda
1.2 Immediate Fabric: Virtual Architecture for Circuit Portability and Fast Placement and Routing.
   James Coole and Greg Stitt
1.3 An Elastic Software Cache with Fast Prefetching for Motion Compensation in Video Decoding.
   Ping Chao and Youn-Long Lin

Session 1B: Reconfigurable and Real-time Systems
Session chair: Sudarshan Banerjee
Session co-chair: Pai Chou
1.1 Verification of Dynamically Reconfigurable Embedded Systems by Model Transformation Rules.
   Felix Madlener, Julia Weingart and Sorin A. Huss
1.2 Hardware/Software Optimization of Error Detection Implementations for Real-time Embedded Systems.
   Adrian Lifa, Petru Eles, Zebo Peng and Viacheslav Izosimov
1.3 Scheduling Garbage Collection in Real-time Systems.
   Martin Kero and Simon Attama
1.4 (S) Components: Platforms and Resources for Work on a Composable, Parallel System.
   Sebastian Buchwald and Andreas Zwickau

Session 1C: Verification & Synthesis
Session chair: Edward Lee
1.1 Automatic Verification of Control System Implementations.
   Adolfo Anta, Rupak Majumdar, Indranil Saha and Paulo Tabuada
1.2 Switching Logic Synthesis for Reachability.
   Ankur Talal and Ashish Tiwari
1.3 Online Dynamic Stability Verification Using Sector Search.
   Cristiano Miranda, Antoniu Pop, Philippe Dumont, Albert Cohen and Marc Duranton
1.4 Component Selection by Graph Transformation.
   Sebastian Buchwald and Andreas Zwickau
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<th>Session 2: Applications and Tools</th>
<th>Session chair: Rodric Rabbah</th>
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<tbody>
<tr>
<td>2.1 Parallelizing the H.264 Decoder on the Cell BE Processor.</td>
<td>Yongjin Cho, Seungkyun Kim, Jaejin Lee and Heonshik Shin</td>
</tr>
<tr>
<td>2.2 Optimal WCET-Aware Code Selection for Scratchpad Memory.</td>
<td>Hui Wu, Jingling Xue and Sri Parameswaran</td>
</tr>
<tr>
<td>2.3 (S) A Model Based Approach for Debugging Embedded Systems in Real Time.</td>
<td>Padma Iyenghar, Clemens Westerkamp, Juergen Wuebbelmann and Elke Pulvermueller</td>
</tr>
<tr>
<td>2.4 (S) PinaVM: a SystemC Front-End Based on an Executable Intermediate Representation.</td>
<td>Kevin Marquet and Matthieu Moy</td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>Session 2: Special session -- Embedded Systems for Future Medical Care</th>
<th>Session chair: Vincent J. Mooney</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 Routing-Based Synthesis of Digital Microfluidic Biochips.</td>
<td>Elena Maftei, Paul Pop and Jan Madsen</td>
</tr>
<tr>
<td>2.2 Mosaic of Organic Development Through Technology Intervention in the Rural Indian Context.</td>
<td>Pingali Rajeswarii and P. Niranjana (invited)</td>
</tr>
<tr>
<td>2.3 The Virtual Hospital.</td>
<td>Danny Petrasek, M.D. (invited)</td>
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<tr>
<td>2.4 Parsimonious Information Technologies for Pixels, Perception, Wetware and Simulation</td>
<td>Alan Barr (invited)</td>
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<thead>
<tr>
<th>Session 2A: Special Session - From ESL-2010 to ESL-2015</th>
<th>Session chairs: Adam Donlin (Xilinx) and Karam Chatha (Arizona State University)</th>
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</thead>
<tbody>
<tr>
<td>ESL and Modeling: Time to Get Rid of the Duct Tape and Bailing Wire.</td>
<td>Tor Jeremiassen, Texas Instruments.</td>
</tr>
<tr>
<td>Putting Virtual Prototypes Into Action,</td>
<td>Tim Koegel, Synopsys.</td>
</tr>
<tr>
<td>ESL Analysis, Verification and Synthesis of SoCs,</td>
<td>Andres Takach, Mentor Graphics</td>
</tr>
<tr>
<td>ESL 2015: The inevitable move to software programmability.</td>
<td>Grant Martin, Tensilica.</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Session 2B: Special Session - HW/SW Co-design for High Performance Computing: challenges and opportunities</th>
<th>Session chairs: X. Sharon Hu (Notre Dame) and Richard Murphy (Sandia)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A new era of HPC System Design.</td>
<td>Sudip Dosanjh, Sandia National Labs</td>
</tr>
<tr>
<td>Who were the enemies of high-performance computing system design in the past 20+ years?</td>
<td>Stephen Poole, US DoE/DoD</td>
</tr>
<tr>
<td>HW/SW Specialization for Heterogeneous Parallelism.</td>
<td>Kunle Olukotun, Stanford University</td>
</tr>
<tr>
<td>Research/funding opportunities in codesign for HPC systems.</td>
<td>Bill Harrod, DARPA</td>
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</tbody>
</table>

**POSTER SESSION @ 14:30**
Session 3: Architectures
Session chair: Aviral Shrivastava

3.1 Implementing Virtual Secure Circuit Using A Custom-Instruction Approach.
Zhimin Chen, Ambuj Sinha and Patrick Schaumont

3.2 Mighty-Morphing Power-SIMD.
Ganesh Dasika, Mark Woh, Sangwon Seo, Trevor Mudge, Nathan Clark and Scott Mahlke

3.3 Towards Minimizing Reconfiguration Overhead in Dynamically Reconfigurable Processors: REDEFINE as a case study.
Ratna Krishnamoorthy, Keshavan Varadarajan, Ganesh Garga, Mythri Alle, Ranjani Narayan, Masahiro Fujita and S. K. Nandy

Session 3A: Optimising Multiprocessor and NoC Platforms for Performance, QoS, and Reliability
Session chair: Rainer Dömer
Session co-chair: Frank Vahid

Jaume Joven, Andrea Marongiu, Federico Angiolini and Luca Benini

3.2 Optimal Synthesis of Latency and Throughput Constrained Pipelined MPSoCs Targeting Streaming Applications.
Haris Javaid, Xin He, Aleksander Ignjatovic and Satish Parameswaran

3.3 OE+IOE: A Novel Turn Model Based Fault Tolerant Routing Scheme for Network-on-Chip.
Sudeep Patil, Yong Zou, Dan Conlin, Scott Mahlke and Ayan Nandy

Session 3B: Power-Aware Design
Session chair: Sarma Vrudhula
Session co-chair: Naehyuck Chang

3.1 Power Aware SID-based Simulator for Embedded Multicore DSP Subsystems.
Cheng-Yen Lin, Po-Yu Chen, Chun-Kai Tseng, Chung-Wen Huang, Chia-Chieh Weng, Chi-Bang Kuan, Shih-Han Lin, and Jenq-Kuen Lee

3.2 Accurate Online Power Estimation and Automatic Battery Behavior Monitoring.
Terry Chang, Weiqiang Zhan, Zhiyin Zheng, Bingyi Xin, Alexander Gunther, Hans-Joachim Klein, Keshavan Varadarajan, and Michael Ruhl

3.3 Statistical Approach in a System Level Methodology to Deal With Process Variation in a System.
Concepción Sanz, Manuel Prieto, José Ignacio Gómez, Christian Franck, and Franky Cathoor

Session 3: Scheduling & Optimization
Session chair: Alessandro Pinto

Jinkyu Lee, Arvind Easwaran, Gang Yao, Xiuyi Zhan and Yunhao Liu

3.2 Load-Based Schedulability Analysis of Certifiable Mixed-Criticality Systems.
Haohan Li and Sanjoy Barua

3.3 Reducing Slack with intra-task Resource Sharing.
Hakan Li and Sanjoy Barua

Room: Kierland 1C
Room: Kierland 1A
Room: Kierland 1B
Room: Kierland 1D
<table>
<thead>
<tr>
<th>EMSOFT</th>
<th>CASES</th>
<th>CODES + ISSS</th>
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</thead>
<tbody>
<tr>
<td>Room: Kierland 1C</td>
<td>Room: Cushing</td>
<td>Room: Kierland 1A</td>
</tr>
<tr>
<td>Session 4: Automotive &amp; Wireless Sensor Networks</td>
<td>Session 4: Architectures</td>
<td>Session 4B: Memory and Communication Architecture</td>
</tr>
<tr>
<td>Session chair: Ken Butts</td>
<td>Session chair: Lothar Thiele</td>
<td>Session chair: Sundeep Pasricha</td>
</tr>
<tr>
<td>4.1 Modeling Buffers with Data Refresh Semantics in Automotive Architectures.</td>
<td>4.1 Implementing Dynamic Implied Addressing Mode for Multi-Output Instructions.</td>
<td>4.1 Automatic Memory Partitioning: Increasing Memory Parallelism via Data Structure Partitioning.</td>
</tr>
<tr>
<td>Linh Thi Xuan Phan, Reinhard Schneider, Samarjit Chakraborty and Insup Lee</td>
<td>Jonghee M. Youn, Jongwon Lee, Yunheung Paek, Jongwung Kim and Jeonghun Cho</td>
<td>Nadav Rotem and Yosi Ben Asher</td>
</tr>
<tr>
<td>4.2 Schedulability and End-to-end Latency in Distributed ECU Networks: Formal Modeling and Precise Estimation.</td>
<td>4.2 Real-time Unobtrusive Program Execution Trace Compression Using Branch Predictor Events.</td>
<td>4.2 Towards a Synthesis Semantics for SystemC Channels.</td>
</tr>
<tr>
<td>A. C. Rajeev, Swarup Mohalik, Manoj G. Dixit, Devesh B. Chokshi and S. Ramesh</td>
<td>Vladimir Uzelac, Aleksandar Milenkovic, Martin Burtscher and Milena Milenkovic</td>
<td>Kim Grüttner, Henning Kleen, Frank Oppenheimer, Achim Rettberg and Wolfgang Nebel</td>
</tr>
<tr>
<td>4.3 (S) TeleScribe: A Scalable, Re-summable Wireless Reprogramming Approach.</td>
<td>4.3 A Memory Interface for Multi-Purpose Multi-Stream Accelerators.</td>
<td>4.3 Demand-based Block-level Address Mapping in Large-scale NAND Flash Storage Systems.</td>
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<tr>
<td>Min-Hua Chen and Pai Chou</td>
<td>Sylvain Girbal, Olivier Temam, Sami Yehia, Hugues Berry and Zheng Li</td>
<td>Zhiwei Qin, Yi Wang, Duo Liu and Zili Shao</td>
</tr>
<tr>
<td>4.4 (S) Nucleos: a Runtime System for Ultra-Compact Wireless Sensor Nodes.</td>
<td>4.4 Hardware-Based Data Value and Address Trace Filtering Techniques.</td>
<td>Adam Hartman, Donald Thomas and Brett Meyer</td>
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<td>Jiwon Hahn and Pai Chou</td>
<td>Vladimir Uzelac and Aleksandar Milenkovic</td>
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</tbody>
</table>

**POSTER SESSION @ 10:00**
5.1 Improving Scratchpad Allocation with Demand-Driven Data Tiling.
Li Wang, Xuejun Yang, Jingling Xue, Tao Tang, Xiaoguang Ren and Shen Ye

5.2 Fine-grain Dynamic Instruction Placement for L0 Scratch-pad Memory.
Jongsoo Park, James Balfour and William Dally

5.3 Improved Procedure Placement for Set Associative Caches.
Yun Liang and Tulika Mitra

5.4 Minimizing Inter-Task Interference.
Lovic Gauthier, Tohru Ishihara, Hideki Takase and Hiroaki Takase

Session 5A: Embedded Tutorial - An Introduction to the SystemC Synthesis Subset Standard
Session Chairs: Philippe Coussy, Université de Bretagne-Sud
Achieving high-quality hardware results using SystemC synthesis.
Mike Meredith, Forte Design Systems
Synthesizing systems containing both algorithmic and control blocks from high-level SystemC specifications using HLS.
Andres Takach, Mentor Graphics
SystemC synthesizability at the pin and transaction levels.
Mike Meredith, Mentor Graphics

Session 5B: Compilation techniques for CGRAs: Exploring all parallelization approaches
Session chair: Tom Vander Aa (IMEC)
Polymorphic pipeline arrays, expanding coarse-grained arrays beyond innermost loops.
Scott Mahlke, University of Michigan
Memory-aware compilation techniques for coarse-grained arrays.
Philipppe Coussy, Université de Bretagne-Sud
Introduction to high-level synthesis of coarse-grained arrays.
Raghu Pasupathy, University of Arizona

Session 5: Flash Memory
Session chair: Dimitrios Soudris

5.1 Using NAND Flash Memory for Executing Large Volume Real-Time Programs in Automotive Embedded Systems.
Yun-Han Chang and Te Wei Kuo
5.2 A Reliable MTD Design for MLC Flash Memory.
Hong Kwon, Eunsam Kim, Jong-Guoo Lee
5.3 Improving Procedure Placement for Set Associative Caches.
Hee Chul Bong, Ye and Sam H. Noh
5.4 Minimizing Inter-Task Interference.
Lovic Gauthier, Tohru Ishihara, Hideki Takase and Hiroaki Takase

EMSOFT 2010
Es Week 2010
Tuesday, October 26, 2010
13:00 - 15:00
Session 6A: Memory architecture for embedded systems
Session chair: Joerg Henkel
Session co-chair: Andy Pimentel
6.1 Dynamic, Non-Linear Cache Architecture for Power-Sensitive Mobile Processors.
Garo Bournoutian and Alex Orailoglu
Hassan Ghasemzadeh and Roozbeh Jafari
6.3 High Durability in NAND Flash Memory through Effective Page Reuse Mechanisms.
Kwangyoon Lee and Alex Orailoglu

Session 6B: New Design Approaches for Network-on-Chip Systems
Session chair: Sundeep Pasricha
Session co-chair: Kees Goossens
6.1 A Holistic Approach to Network-on-Chip Synthesis.
Glenn Leary and Karam Chatha
6.2 NeuroNoC: Neural Network Inspired Runtime Adaptation for an On-chip Communication Architecture.
Thomas Ebi, Mohammad Abdullah Al Faruque and Jörg Henkel
Paul Bogdan and Radu Marculescu
6.4 Mini panel.
Moderator: Petru Eles

Session 6: Distribution & Event Graphs
Session chair: Walid Taha
6.1 A Unifying View of Loosely Time-Triggered Architectures.
Albert Benveniste, Anne Bouillard and Paul Caspi
6.2 Semantics-Preserving Implementation of Synchronous Specifications over Dynamic TDMA Distributed Architectures.
Dumitru Potop-Butucaru, Akramul Azim and Sebastian Fischmeister
6.3 (S) From High-level Component-Based Models to Distributed Implementations.
Borzoo Bonakdarpour, Marius Bozga, Mohamad Jaber, Jean Quilbeuf and Joseph Sifakis
Thomas Huining Feng, Edward A. Lee and Lee W. Schruben

Session 6: Special Session: IEEE McDowell Lecture and Novel Architectures
Session chair: Vinod Kathail/Reid Tatge
6.1 Compilers, Architectures and Synthesis for Embedded Computing: Retrospect and Prospect.
Prof. Krishna Palem
6.2 Optimizing Energy to Minimize Errors in Dataflow Graphs Using Approximate Adders.
Zvi Kedem, Vincent Mooney, Kirthi Krishna, Krishna Palem, Avani Devarasetty and Phanideepak Parasuramuni
6.3 High Durability in NAND Flash Memory through Effective Page Reuse Mechanisms.
Kwangyoon Lee and Alex Orailoglu

Session 6: POSTER SESSION @ 17:00
Session 7A: Novel Techniques for Accelerating System Simulation

Session Chair: 
Session Co-Chair: 
7.1 parSC: Synchronous Parallel System Simulation on Multi-Core Architectures. 
Christoph Schumacher, Rainer Leupers, Dietmar Petras and Andreas Hoffmann

7.2 FastFwd: An Efficient Hardware Acceleration Technique for Trace-driven Network-on-Chip Simulation. 
Krishnaiah Gummidipudi, B.V.N Silpa, Preeti Ranjan Panda and Anshul Kumar

7.3 FEMU: A Firmware-Based Emulation Framework for SoC Verification. 
Hao Li, Dong Tong, Kan Huang and Xu Cheng

Daniel Cordes, Peter Marwedel and Arindam Mallik

7.2 Performance Modeling of Embedded Applications with Zero Architecture Information. 
Srinivasan Parthasarathy and Fabrizio Ferrandi

7.3 Performance Modeling of Embedded Applications with Zero Architecture Information. 
Srinivasan Parthasarathy and Fabrizio Ferrandi

Session 7.2: Embedded Software Performance Optimization

Session Chair: Aviral Shrivastava
Session Co-Chair: Preeti Ranjan Panda
7.1 Automatic Parallelization of Embedded Software Using Hierarchical Task Graphs and Integer Linear Programming. 
Daniel Cordes, Peter Marwedel and Arindam Mallik

7.2 Performance Modeling of Embedded Applications with Zero Architecture Information. 
Srinivasan Parthasarathy and Fabrizio Ferrandi

Amrit Panda, Nikhil Ghadge, Anuruddha Kadne and Karim Michael Jantz and Prasad Kulkarni

7.4 Design Space Exploration of the Embedded System with an Application Case-Study. 
Kiran Kumar

Session 7.3: Model-Based Design & Patterns

Session Chair: Lothar Thiele
Session Co-Chair: 
7.1 Model-Based Implementation of Real-Time Applications. 
Tesnim Abdou, Jacques Combes and Karam Chatha

7.2 Model-Based Specification of Timing Requirements. 
Christian Buchli, Rina Caponera, Alios Kroll and Michael Ciesielski

7.3 Initiating a Design Pattern Catalog for Embedded Network Systems. 
Sally K. Wahba, Jason O. Hallstrom and Neelam Soundarajan

Session Chair: Tulika Mitra
Session Co-Chair: 
7.1 Eliminating False Parallelization Phases in the Development of Code. 
Marilyn Wolf and Hyesoon Kim

7.2 Practical Aggregation of Semantic Program Properties for Machine Learning Based Compilation. 
Mircea Namolaru, Albert Cohen, Grigori Fursin, Michael Jantz and Prasad Kulkarni

7.3 Design Space Exploration of the Turbo Decoding Algorithm on the NVIDIA GPU. 
Dongwon Lee, Martyn Wolf and Xu Cheng
### Session 8: Scheduling & Control

#### 8.1 Power-Aware Temporal Isolation with Variable-Bandwidth Servers
Silviu Craciunas, Christoph Kirsch and Ana Sokolova

#### 8.2 Resource Adaptations with Servers for Hard Real-Time Systems
Nikolay Stoimenov, Lothar Thiele, Luca Santinelli and Giorgio Buttazzo

#### 8.3 (S) Energy-Aware Packet and Task Co-Scheduling for Embedded Systems
Luca Santinelli, Mauro Marinoni, Francesco Prosperi, Francesco Esposito, Gianluca Franchino and Giorgio Buttazzo

#### 8.4 (S) Dynamic Tuning of Feature Set in Highly Variant Interactive Applications
Tushar Kumar, Romain Cledat and Santosh Pande

### Session 8A: Reliability and Memory Issues in MPSoCs

#### 8.1 System-Level Reliability Modeling of MPSoCs
Yun Xiang, Thidapat Chantem, Robert Dick, Sharon Hu and Li Shang

#### 8.2 A Task Re-Mapping Technique for Reliable Multi-core Embedded Systems
Chanhee Lee, Hokeun Kim, Hae-woo Park, Sungchan Kim, Hyunok Oh and Soonhoi Ha

#### 8.3 Heap Data Management for Limited Local Memory (LLM) Multi-core Processors
Ke Bai and Aviral Shrivastava

### Session 8B: Special Session - Unconventional Fabrics, Architectures, and Models for Future Multi-core Systems

#### Self-assembled Nanoscale On-Chip Interconnect: The Good, the Bad and the Ugly
Christof Teuscher, Portland State University

#### Small-World Hybrid Wireless Network-on-Chip Architecture for Massive Multi-Core Systems
Partha Pande, Washington State University

#### Is the Network the Real Problem for Future Multi-core Systems?
Radu Marculescu, CMU

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**POSTER SESSION @ 14:30**

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<tr>
<td>Session 8: Cache and Memory Architectures Session chair: Oliver Bringmann</td>
<td>Session 8A: Reliability and Memory Issues in MPSoCs Session co-chair: Paul Pop</td>
<td>Session 8A: Reliability and Memory Issues in MPSoCs Session chair: Aseem Gupta</td>
<td>Session 8B: Special Session - Unconventional Fabrics, Architectures, and Models for Future Multi-core Systems Session chair: Radu Marculescu</td>
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ESWEEK Industrial PANEL

Wednesday, Oct. 27th 2010
15:30

The future of embedded architectures

Organizers: Wolfgang Rosenstiel, Karamvir S. Chatha

Moderator: Alberto L Sangiovanni-Vincentelli

Panelists:
~ Pranav Mehta
  Senior Principal Engineer and Chief Technology Officer of Intel's Embedded and Communications Group
~ Nat Seshan
  Distinguished Member Technical Staff, Director of DSP Architecture, Texas Instruments
~ Grant Martin
  Chief Scientist, Tensilica Inc.
~ Jim Holt
  Manager, Processor Core Architecture and Modeling, Networking and Multimedia Group, Freescale Inc.
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