ENHANCING THE RELIABILITY OF STT-RAM THROUGH CIRCUIT AND SYSTEM LEVEL TECHNIQUES

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ABSTRACT

Spin torque transfer random access memory (STT-RAM) is a promising memory technology because of its fast read access, high storage density, and very low standby power. These memories have reliability issues that need to be better understood before they can be adopted as a mainstream memory technology. In this paper, we first study the causes of errors for a single STT memory cell. We see that process variations and variations in the device geometry affect their failure rate and develop error models to capture these effects. Next we propose a joint technique based on tuning of circuit level parameters and error control coding (ECC) to achieve very high reliability. Such a combination allows the use of weaker ECC with smaller overhead. For instance, we show that by applying voltage boosting and write pulse width adjustment, the error correction capability (t) of ECC can be reduced from t=11 to t=3 to achieve a block failure rate (BFR) of 10^{-9}.

***Keywords*:** Spin torque transfer RAM (STT-RAM), bit error rate, process variation, circuit level techniques, error control coding

1. INTRODUCTION

Over the last decade, there has been significant effort in designing different types of memory devices that have high data storage density and low leakage power. Many of these works focus on finding an alternative to commonly used SRAM, DRAM and Flash memories [1-2]. One of the promising candidates is Spin Torque Transfer RAM (STT-RAM) [3-5] because of its fast read/write operation, very low standby power and high endurance. Unlike SRAM or DRAM where data is stored as charge, in STT-RAM, data is stored as a resistance value which is a function of the magnetization angle of the magnetic tunneling junction (MTJ). There are two states based on whether the direction of the magnetization angle is parallel (bit '0') or antiparallel (bit '1').

Majority of the errors for a STT-RAM cell are due to process variations [6-8]. These include variation of the access transistor sizes (W/L), variation in V_{th} due to random dopant fluctuation (RDF), MTJ geometric variation and initial angle of the MTJ. The effect of access transistor on system performance has been investigated in [4], [6]. Errors due to these variations can be as high as 10^{-1} for write-1 operation [6]. Fortunately, the error rate can be dropped to $< 10^{-5}$ by tuning circuit parameters such as W/L ratio of the access transistor, changing the current pulse width during write and increasing the voltage across the STT-RAM cell.

In this work, we first study the causes of errors STT-RAM starting from first principles and model the probability of errors. In each case, we show how circuit-level techniques can reduce some of the errors. Next, we show how traditional error control coding (ECC) techniques can be used in conjunction with circuit-level techniques to further improve the error rate. For instance, we show that by applying a combination of write-pulse width adjustment and voltage boosting at the circuit level followed by a BCH code based ECC scheme at the system level, we can achieve a block failure rate (BFR) of 10^{-9}. We compare the performance of different candidate schemes along with their hardware overhead and show that the proposed method has much lower cost. The specific contributions of this paper are as follows:

- An accurate model of an STT-RAM cell based on energy interaction.
- A detailed study of process variation induced failures in STT-RAM.
- Development of circuit level techniques for STT-RAM that reduce the error rate due to judicious use of increase in W/L ratio of the access transistor, higher voltage difference across the memory cell and pulse width adjustment in write operation.
- Evaluation of the performance and hardware overhead of the different ECC-based schemes.

The rest of the paper is organized as follows. Section 2 describes the basics of STT-RAM cell operation along with an accurate physical model. Section 3 describes the causes of read/write failures in an STT-RAM cell. Section 4 proposes circuit parameter tuning to address these errors. Section 5 focuses on BCH based ECC schemes along with the synthesis results. The conclusion is given in section 6.

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2. BACKGROUND

In STT-RAM, the resistance of the magnetic tunneling junction (MTJ) determines the logical value of the data that is stored. MTJ consist of a thin layer of insulator (spacer-MgO) about ~1nm thick sandwiched between two layers of ferromagnetic material [3]. Magnetic orientation of one layer is kept fixed and an external field is applied to change the orientation of the other layer. Direction of magnetization angle (parallel (P) or anti-parallel (AP)) determines the resistance of MTJ which is translated into storage; parallel corresponds to storage of bit '0' and anti-parallel corresponds to storage of bit '1'. Low resistance (parallel) state corresponds to the case when magnetic orientation of both layers is in the same direction. By applying external field higher than critical field, magnetization angle of free layer is flipped by 180^0 which leads to a high resistance state (anti-parallel). The difference between the resistance values of parallel and anti-parallel states is called tunneling magneto-resistance (TMR) which is defined as $TMR = \frac{(R_{AP}-R_P)}{R_P}$ where R_{AP} and R_P are the resistance values at anti-parallel and parallel states. Increasing the TMR ratio increases the separation between states and improves the reliability of the cell [5]. Figure 1 describes the cell structure of an STT-RAM and highlights the parallel and anti-parallel states.

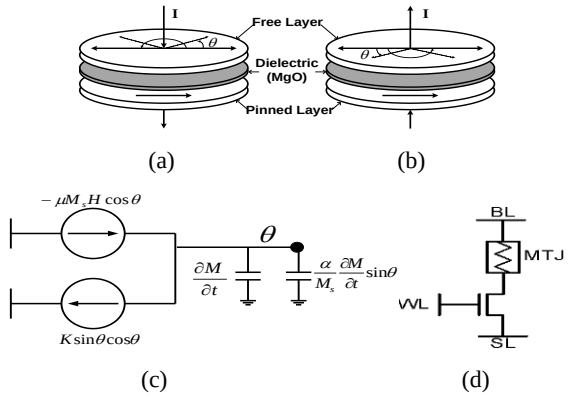


Figure 1. STT-MRAM structure (a) Parallel, (b) Anti-parallel, (c) MTJ circuit structure based on the energy equations, (d) STT-RAM circuit structure.

Physical Model: A physical model of MTJ based on the energy interaction is presented. Magnetization angle of the free layer is determined based on the dimensions of MTJ and the external field applied. Energies acting in MTJ are Zeeman, anisotropic and damping energy [9]. These energy types determine the change in magnetic orientation, alignment of the magnetization angle along the fixed axis and are used to form the LLG (Landau–Lifshitz–Gilbert) equation. The stable state of MTJ corresponds to minimum total energy. State change of MTJ cell can be derived by combining these energy types:

$$\frac{d\vec{M}}{dt} = -\mu_0 \cdot M_s \cdot \vec{H} + \frac{\alpha}{M_s} \cdot \vec{M} \times \frac{d\vec{M}}{dt} + Ksin\theta cos\theta$$

where $\vec{M}$ is magnetic moment, μ_0 is vacuum permeability, α is damping constant.

The energy equation can be modeled using Verilog-A to simulate the circuit characteristics of STT-RAM as illustrated in Figure 1(c). For instance, differential terms are modeled using capacitance while Zeeman and damping energy are described by voltage dependent current source. The voltage of the capacitor indicates the evaluated state (magnetization angle) which is further translated to resistance of MTJ. Figure 2 shows the hysteresis curve of STT-MRAM which have been validated with published data from [10, 11].

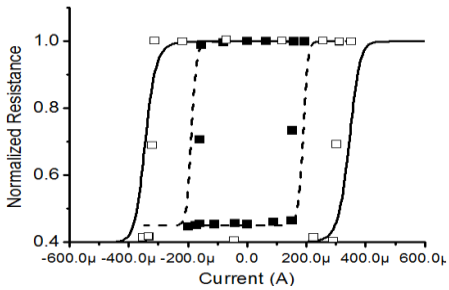


Figure 2: Hysteresis effect predicted by model validated by experimental data [10, 11]

Read/Write Operation: The STT-RAM cell structure consists of an access transistor in series with the MTJ resistance, as illustrated in Figure 1(d). The access transistor is controlled through WL, and the voltage levels used in bit line (BL) and select line (SL) lines determine the current which is used to adjust the magnetic field. There are three modes of operation: write-0, write-1 and read. We distinguish between write-0 and write-1 because of the asymmetry in their operation. In general, direction of the current during write-0 and read operation are the same, while the magnitude of the current is fairly high (approximately 10X) during the write operation. For read operation, current lower than critical current is applied to MTJ to determine its resistance state. Low voltage (~0.1V) is applied to BL, and SL is set to ground. When the access transistor is turned on, a small current passes through MTJ whose value is detected based on a conventional voltage sensing or self-referencing schemes [12]. During write operation, BL and SL are charged to opposite values depending on bit value that is to be stored. During write-0, BL is high and SL is set to zero, whereas during write-1, BL is set to zero and SL is set to high. The asymmetric structure of write-0 and write-1 operations motivates operating SL higher voltage than nominal during write-1 so that both operations generate comparable write-current. Such a circuit technique will be described later.

3. Error Model

3.1 Variation in Device Parameters

There are several factors that affect the failure in STT-RAM memories: access transistor manufacturing errors such as those due to random dopant fluctuations (RDF), channel length, and width modulations, geometric variations in MTJ such as area and thickness variation, and initial magnetization angle variation [8]. Note that all these variations cause hard errors. Apart from errors that are caused by process variations, MTJ also suffers from time dependent reliability issues. MTJ structure consists of a very thin insulating layer (~1nm) and voltage across MTJ can be approximately 0.6V-1V. This results in a very high electric field across the thin insulator (~10MV/cm) which can cause time dependent dielectric breakdown (TDDB) [13]. With high scaling, the electric field across insulating layer rises, thereby increasing the possibility of TDDB.

Next we consider the effect of key process variation factors on the error rate. The effect of RDF on threshold voltage is typically modeled with an additive iid Gaussian distribution. Variance of threshold voltage of a MOSFET is proportional to $\sigma_{VT} \sim \frac{EOT}{\sqrt{L_t \times W_t}}$, where EOT is oxide thickness, and L_t and W_t are length and width of the transistor, respectively. For 32nm, σ_{VT} is approximately between 40 to 60mV [14]. We model CMOS channel length and width variation using iid Gaussian distribution with 5% variation. These variations induce change in the drive current of the transistor which results in increase on variation in both read and write operation. We consider 40mV variation for RDF when transistor width is 128nm which is equivalent to W/L=4 and scale it for different W/L ratios. Variation in tunneling oxide thickness ($t_{ox(MTJ)}$) and surface area (A_{MTJ}) of MTJ are the main causes behind the resistance change in MTJ material. Resistance of the MTJ is proportional to $(1/A_{MTJ})e^{t_{ox(MTJ)}}$ [6]. In our simulations, we set the nominal values of (R_P) to 2.25K and (R_{AP}) to 4.5K and modeled the variations using iid Gaussian distribution with 2% variance for thickness and 5% variance for the area [6]. Furthermore, initial magnetization angle of the MTJ affects the duration of the write operation, since it induces extra resistance when the angle is not aligned properly at the initial state. This parameter is a consequence of the thermal fluctuation of the MTJ. Such a variation is also modeled using iid Gaussian distribution with 0.1 radian variance [5]. The nominal values and variance of the device parameters are listed in Table 1.

Table 1. STT-RAM Device parameters.

	Nominal	Variance
Channel Length(nm)	32	5%
Channel Width (nm)	96,128,160	5%
Threshold (RDF)	0.4V	σ_{VT}=40mV
R_P (Parallel)	2.25K	~6%
R_{AP} (Anti-parallel)	4.5K	~6%
MTJ Initial Angle	0	0.1π

3.2 Errors in read and write operations

The reliability of an STT-RAM cell has been investigated by several researchers. While [5] studied the failure rate of a single STT-RAM cell using basic models for transistor and MTJ resistance, process variation effects such as RDF and geometric variation were considered in [6][15]. In this section, we also present the effects of process variation and geometric variation both for read and write operation and present the contribution of each variation on the overall BER. We add the variation effects to the nominal Hspice model of STT-RAM and use Monte Carlo simulations to generate the error rates caused by each variation.

Read Operation: During read operation BL is set to 0.1V, SL is set to ground and the stored value is determined based on the current passing though the MTJ. Threshold current value is used to distinguish between 2 states (read-0 and read-1). Typically there are two main types of failures that occur during the read operation: read disturb and false read. Read disturb causes the value stored in the MTJ to be flipped because of large current during read. False read occurs when current of parallel (anti-parallel states) crosses the threshold value of the anti-parallel (parallel) state. In our analysis we find that the false read errors are dominant during the read operation, thus, focus on the false reads in the error analysis.

Write Operation: During write-0, BL is high and SL is set to zero whereas during write-1 BL is set to zero and SL is set to high. Figure 3 illustrates the write-0 and write-1 time distribution of an STT-RAM cell when access transistor size is W/L=4. We see that both distributions have long tails unlike Gaussian distributions. Failures occur when the distribution of write latency crosses the predefined access time as illustrated in Figure 3. Write-1requires longer latency and is more prone to errors. During write-1, access transistor and MTJ pair behaves similar to a source follower which increases the voltage level at the source of the access transistor and reduces the driving write current.

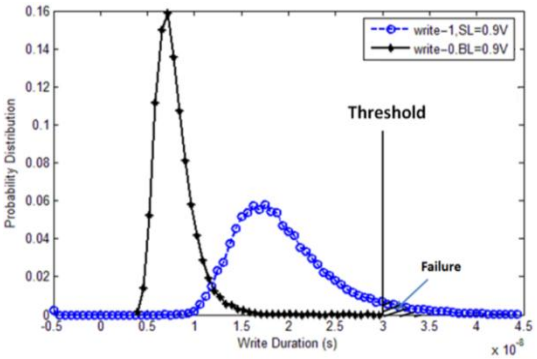


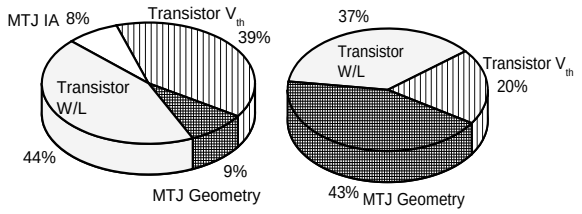
Figure 3. Distribution of write time during write-0 and write-1. Failure occurs when the distribution crosses the threshold value.

Table 2 shows BER for read and write operations of STT-RAM at nominal conditions corresponding to V_{dd}=0.9V, write pulse =30ns, V_{read}=0.1V and access transistor size of W/L=4. Write-1 has very high BER compared to write-0 which has a BER of 10^{-6}. The effect of such asymmetry in write operation was also presented in [6][15].

Table 2. Bit error rates of a single STT-RAM cell.

Read (Vread = 0.1V)		Write (pulse width = 30ns)	
0	1	0	1
$\sim 10^{-5}$	$\sim 10^{-5}$	$\sim 2 \times 10^{-6}$	$\sim 3 \times 10^{-2}$

The variation impacts of the different parameters are presented in Figure 4 for read and write operations. To generate these results, we changed each parameter one at a time and did Monte Carlo simulations to calculate the contribution of each variation on the overall error rate. We see that variation in access transistor size is very effective in shaping the overall reliability. It affects the read operation by 37% and write by 44%; write-0 and write-1 have similar trends. The threshold voltage variation affects the write operation more than the read operation. Finally, the MTJ geometry variation is more important in determining the read error rate as illustrated in Figure 4(b) – a factor that should be taken into account in the design of read intensive memories.



(a) (b)

Figure 4. Effects of different variations on STT-MRAM. (a) Write operation, (b) Read operation.

4. CIRCUIT-LEVEL TECHNIQUES TO REDUCE ERROR

In this section we show how voltage boosting, write pulse width adjustment and access transistor W/L sizing can be used to improve the reliability of the STT-RAM cell. In [5][6], effect of access transistor sizing and process variation on reliability and energy consumption has been studied. In addition, [15] also studied the effect of write pulse width and process variation on reliability. In our work, we consider the joint effect of write pulse width adjustment and voltage boosting to improve reliability with lower overhead.

4.1 Effect of W/L of access transistor

The width of the access transistor has two effects on the read current distribution: it reduces the effect of RDF variation and improves the reliability by increasing the distance between the mean of the read-0 and read-1 distributions. Based on the W/L ratios we can choose the threshold value that maximizes the detection probability during read operation, which in return minimizes the BER. For instance, when W/L=3, BER=0.7×10^{-4} ; it reduces to BER=0.25×10^{-5} when the size W/L increases to 5. Even though increasing W/L improves the reliability for the read operation, it reduces the cell density and increases the power consumption. Similarly, when W/L ratio of the access transistor increases, its current driving capability increases which in return reduces the necessary time duration for a successful write operation. Figure 5 illustrates this phenomenon by plotting the write latency distributions for three W/L ratios of the access transistor.

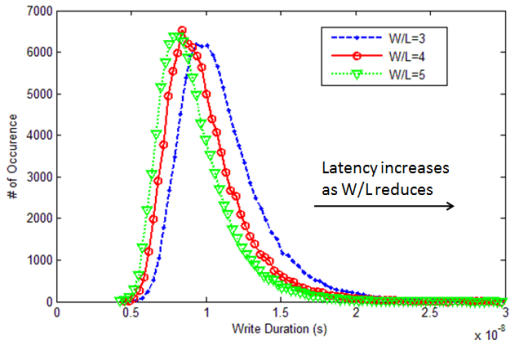


Figure 5. Distribution of write-0 latency for different access transistor sizes

4.2 Effect of voltage boosting and write pulse width duration

Gate level (WL) voltage boosting has been investigated in [20] to reduce the write-1 latency of STT-RAM. It is an effective way of increasing the drive current of access transistor which leads to reduction in latency. However, WL boosting requires separate word lines for write-0 and write-1 operations. A two step writing, erase/program schemes have been proposed in [20] to overcome the limitations; however all the schemes incur extra latency or energy consumption.
We propose boosting SL during write operation to improve the write-1 reliability. This method enables reduction of the pulse duration for write-1 operation while incurring very small overhead. Moreover it reduces the average latency and variation of the write-1 operation and allows it to have the same latency as the write-0 operation operating at nominal voltage. Figure 6 illustrates the BER of write-1 operation under different voltage levels and write pulse width for access transistor size of W/L=4. As expected, increasing the pulse width reduces the BER for both write-0 and write-1 operations. Furthermore, boosting voltage level of SL during write-1 operation also reduces the write-failures. For instance, when pulse width is 30ns, write-1 BER=0.25×10^{-2} when the SL voltage is 1.1V, whereas write-1 BER=0.4×10^{-4} when the SL voltage is 1.3V.

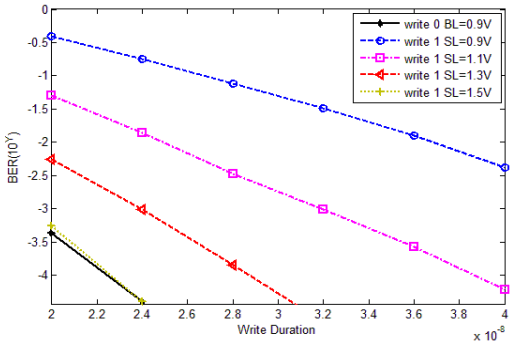


Figure 6. BER vs write pulse duration for different values of SL voltage.

Next we investigate the combination of different write pulse widths and boosted SL voltages that can achieve the same target BER. For BER=10^{-5}, we consider the following combinations of write pulse widths and boosted voltages: (60ns,0.9V), (42ns,1.1V), (31ns,1.3V) and (25ns,1.5V). We see that the average energy consumption of each write operation is comparable and thus combinations with higher voltage levels become more attractive due to lower latency. In such a scenario, the system can use same write pulse width for both write-1 and write-0 operations, thereby simplifying the overall write operation.

We choose the combination of write pulse width of 31ns and SL voltage of 1.3V that achieves BER of ~10^{-5}. Combinations with lower pulse width have higher boosted voltage and may adversely affect the reliability in the long run by increasing the stress that occurs over the dielectric material between two magnetic layers [16]. Combinations with lower voltage have significantly larger write pulse width and would increase the latency and thereby the memory timing performance. Thus simple tuning of circuit parameters can achieve a significant reduction in the BER. However, for reliable memory operations, the target error rate is a lot lower and such error rates are not achievable using only circuit-level techniques. Using only ECC is also very costly. In the following section we describe our approach of applying error control coding on top of circuit-level techniques to achieve a high level of reliability.

5. SYSTEM LEVEL TECHNIQUES

One of the effective techniques to reduce the error rate in memories is through error control coding (ECC). As described in Section 2, raw error rate of STT-RAM can be significantly reduced using circuit level techniques. As a result, strong ECC codes are no longer needed to achieve superior error correction performance and moreover, it reduces the burden of circuit-level techniques.

We consider block failure rate (BFR) as the performance metric since it represents the decoding performance more accurately compared to bit error rate. The block failure rate for a block size N is calculated using a binomial distribution of uniform errors as:

$$BFR = P(error > t) = \sum_{i=t+1}^{N} \binom{N}{i} BER^i (1-BER)^{N-i}$$

where t is the correction strength of the ECC and BER represents the raw error rate after applying circuit-level techniques. We assume N=1024 bits and consider different ECC schemes operating on 64 bits, 256 bits and 1024 bits. The storage overhead of an (n,k) ECC code is defined as $\frac{n-k}{n}$ where k represents the number of information bits for an ECC codeword length of n.

In this paper, the target BFR is set to 10^{-9} which is almost constant over the whole lifetime. Figure 7 illustrates the performance of different ECC schemes, namely, BCH(1145,1024), BCH (1057,1024) and BCH(78,64). We choose BCH(1145,1024) with t=11 since when raw BER=10^{-3} and circuit level techniques are not employed, only this code can achieve the target BFR. When circuit-level techniques are used, a much weaker ECC such as BCH(1057, 1024) with t=3 can achieve the same BFR. We also consider BCH(78, 64) since it has very small latency; unfortunately its storage overhead is quite high (18%).

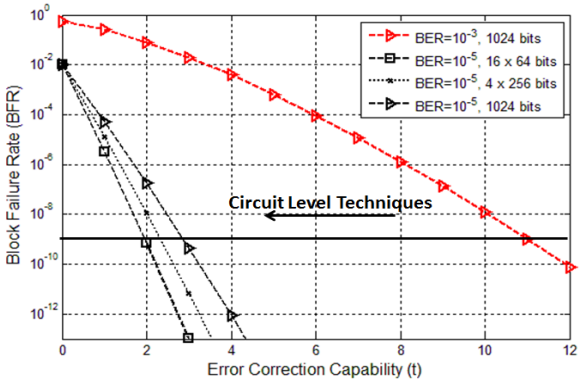


Figure 7: Block failure rate vs ECC correction strength for 1024 bits using various block sizes 64, 256 and 1024

Hardware overhead: The candidate BCH codes for STT-RAM have been synthesized in 45nm technology using Nangate cell library [17] and Synopsys Design Compiler [18]. The synthesis results are listed in Table 3. BCH decoders use pipelined simplified inverse-free Berlekamp-Massey(SiBM) algorithm. The 2t-fold SiBM architecture [19] is used to minimize the circuit overhead of Key-equation solver while its latency is maximized. A parallel factor of 8 is used for all the syndrome calculation and Chien search circuitries. All the power numbers are simulated when the clock period is set to the critical path, which equals to the delay of 1 Galois field multiplier and 1 Galois field adder.

The energy, latency, area and redundancy rate of the candidate ECC schemes for STT-RAM are shown in Table 3. BCH(78, 64) has 18% memory overhead but it improves latency by 20X compared to BCH(1145, 1024). Such high processing speed is beneficial for low level caches. Smaller

Table-3 Hardware overhead of the candidate ECC schemes for STT-RAM.

	Energy (pJ)	Latency(ns)	Area	Extra Storage
BCH(78,64)	2.3 x 16	11.9	1674 x 16	18.0%
BCH(1057,1024)	114.1	195.5	3252	3.1%
BCH(1145,1024)	398.3	211.8	9976	10.5%

BCH also provides energy improvement compared to larger codes since it uses smaller Galois Field multiplication and operations. For instance, 16 BCH(78, 64) provides 3X energy gain compared to single BCH(1057, 1024) and 9X energy gain compared to single BCH(1145, 1024). BCH(1057,1024) has only 3% additional storage and is more favorable for devices that require lower memory overhead.

6. CONCLUSION

In this paper we advocate the joint use of circuit parameter tuning and ECC to improve the reliability of STT-RAM. We first analyze the error sources and build an accurate error model. Next we show that for STT-RAM, the hard error rate can be reduced by tuning the W/L ratios of the access transistors, boosting the voltage and adjusting the write pulse width. For higher reliability, we propose use of weaker ECC in conjunction with the circuit-level techniques. We show that since circuit-level techniques can drop the BER to 10^{-5}, it is sufficient to use a BCH code with only t=3 to achieve a BFR of 10^{-9}. We synthesize the ECC schemes in hardware and show that the hardware overhead, including additional storage, is quite small.

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