

EEE 526: VLSI Architectures (Fall 2010)

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Meeting times: SCOB 201 Mon and Wed 5:00-6:15pm
Office hours: GWC 418 Wed 11:30-12:30pm, Fri 10:00-11:00am

This course focuses on high throughput and low power VLSI architectures for signal processing applications. The prerequisites for this course are Computer Architectures and Digital Signal Processing (400 level).

Selected Topics:

1. Application specific architectures for DSP applications; Systolic arrays (automated mapping procedures); DSP processors; Multi-core architectures.
2. Datapath design and optimization: a brief review of datapath components (fast adders and multipliers); pipelining and parallel processing of digital filters (non-recursive and recursive).
3. High level synthesis: scheduling and allocation algorithms (list-based and force-directed scheduling, ILP).
4. Low power design of digital systems: optimizations at the system-level, algorithm level and architecture level; case studies.
5. Miscellaneous topics (memory design for embedded systems, design issues for battery powered systems, reliable computing, network-on-chip architectures, 3D architectures)

Course Information:

Class Website: <https://myasucourses.asu.edu/>

Text: There is no fixed text for this course. The instructor's notes and relevant papers will be available in the class website. The supplementary texts for this course are as follows. These will be available in the Nobel Science Library (reserve section).

1. Vijay K. Madisetti, *VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis*, IEEE Press.
2. S. Y. Kung, *VLSI Array Processors*, Prentice Hall.
3. K. K. Parhi, *VLSI Digital Signal Processing Systems. Design and Implementation*, Wiley.
4. A. Raghunathan, N. K. Jha and S. Dey, *High-Level Power Analysis and Optimization*, Kluwer Academic Publishers.

Grading: 5-6 homework assignments, 1 term/research paper, 1 midterm exam and 1 comprehensive final exam.

Grading policy: Midterm Exam: 20%, Final: 30%, Term paper: 30%, Class participation: 10% and Homework: 10%.

Other information:

Midterm exam will be held on 20th October and the final exam will be held on 13th December.