

EEE/CSE 120: Digital Design Fundamentals. Fall 2002

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Meeting Times: AG 350. Mon and Wed 11:40 - 12:30pm.

Office hours: GWC 418. Mon and Wed 12:30-1:30pm, Tu: 1:00-2:00pm

Objective: To be able to analyze, design, construct and debug digital combinational logic circuitry and digital finite state machine circuitry.

Text:

1. Alan B. Marcovitz, *Introduction to Logic Design*, McGraw Hill.
2. CD: *Dr. Dan's Digital Design Fundamentals*, Daniel Tylavsky, Dr. Dan's Publishers.

References:

1. Charles H. Roth, *Fundamentals of Logic Design*, PWS Publishing Company.
2. Schaum's Outline Series, *Introduction to Digital Systems*, McGraw Hill.

Grading:

- * 7-8 homework assignments: The lowest homework score will be dropped.
- * Laboratory assignments (5 simulation, 4 hardware, and 1 design project): To pass the course, you need to do at least 3 (out of 4) hardware and 4 (out of 5) simulation laboratory assignments. None of the laboratory scores will be dropped.
- * 2 in-class tests, and 1 comprehensive final exam. A makeup test will only be given for medical reasons.

Grading policy:

Test 1: 15%, Test 2: 20%, Final: 25%, Homework assignments: 10%, Software lab: 12%, Hardware lab: 12%, Design project 6%.

Other information:

- * There will be a problem solving session (optional) every Tuesday from 1:00 - 2:00 pm in GWC 409.
- * Late homework submissions will *not* be allowed. The homework solutions will be placed in the *reserve* section of the Nobel Science Library.
- * The hardware laboratory is located in GWC 273.
- * The software laboratory assignments can be done in any of the IT sites. The TAs will however be available only in GWC 185.
- * The WEB site for this course is <http://www.eas.asu.edu/cse120>. Check this site for announcements etc.

Course Schedule

Aug 26	Number Systems	1.1.1
Aug 28	Binary arithmetic	1.1.2-1.1.4
Sep 4	Boolean Algebra	2.1-2.5
Sep 9	Boolean Algebra	2.7, 2.9, 2.11
Sep 11	Karnaugh maps	2.6, 3.1.1
Sep 16	Karnaugh maps	3.1.2-3.1.4
Sep 18	Adders, Subtracters	4.2
Sep 23	NAND and NOR gate networks	2.8
Sep 25	Review	
Sep 30	Test 1	
Oct 2	ALU and Tristate buffer	Dan's CD, 4.6
Oct 7	Multiplexers and Decoders	4.3-4.5
Oct 9	Combinational circuit design examples	4.8
Oct 14	Timing diagrams	
Oct 16	Flipflops	5.1
Oct 21	Synchronous circuits: analysis	5.3
Oct 23	Synchronous circuits: synthesis	5.2
Oct 28	FSM design examples	5.5, 5.6
Oct 30	FSM design examples	5.7
Nov 4	Registers	6.1
Nov 6	Review	
Nov 13	Test 2	
Nov 18	Counters	6.2
Nov 20	Programmable logic devices	4.7
Nov 25	Microprocessor architecture	Dan's CD
Nov 27	Microprocessor design	Dan's CD
Dec 2	Memory	
Dec 4	Memory systems	Dan's CD
Dec 10	Review	
Dec 18	Final exam (7:40-9:30am in AG350)	