

EEE 525: VLSI Design (Spring 2004)

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Class Meeting: SCOB 201

Meeting hours: 12:15-1:30 pm Tu Th

Office: GWC 418

Office hours: 1:30-2:30 pm Tu Th, 3:00-4:00 pm Wed

The aim of this course is to introduce the student to theoretical as well as practical aspects of Very Large Scale Integrated (VLSI) system design. The specific topics that would be discussed in this course are as follows.

Topics:

1. Introduction – MOSFET transistor, CMOS inverter (static and dynamic behavior), Wire models
2. Designing combinational logic gates in CMOS – static CMOS design, dynamic CMOS design, power consumption
3. Designing sequential logic circuits – flipflops and latches
4. Arithmetic building blocks – adder, multiplier, shifter
5. Memory design – memory core (RAM, ROM), peripheral circuitry
6. Timing issues – clock skew
7. Low power design
8. Coping with interconnect – capacitive, resistive and inductive parasitics
9. Testing – stuck-at faults, design strategies for test

Prerequisite: EEE 425 or equivalent

Course Information:**Text:**

Rabaey, Chandrakasan and Nikolic, *Digital Integrated Circuits. A Design Perspective*, Second Edition, Prentice Hall.

<http://bwrc.eecs.berkeley.edu/lcBook/>

Supplementary Text:

Neil H.E. Weste and Kamran Eshraghian, *Principles of CMOS VLSI Design. A Systems Perspective*, Addison Wesley.

K. Roy and S. C. Prasad, *Low Power CMOS VLSI Circuit Design*, John Wiley.

Laboratory:

The ULSI Laboratory is located in the Brickyard. CAD Tools by Cadence will be used in this course.

Grading: 5-6 homework assignments, 6-7 laboratory assignments, 1 large project, 1 midterm exam and 1 comprehensive final exam.

Grading policy: Midterm Exam: 20%, Final: 25%, Homework assignments: 15%, Laboratory assignments: 10%, Project: 30%.

Exam Schedule: The midterm exam will be held on March 11 and the final exam will be held on May 11.

Teaching Assistants:

Vijay Varadarajan (vijay.varadarajan@asu.edu) is the teaching assistant for this course. His office hours are not known at this time.