

EEE 526: VLSI Architectures (Fall 2003)

Dr. Chaitali Chakrabarti

Class hours: 3:50-5:05 M W

Office hours: 5:15-6:00 M W, 2:00-3:00 Tu

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This course covers theoretical and practical aspects of VLSI architectures. The topics range from application-specific architectures to high level synthesis to low power design to parallel implementations. The prerequisites for this course are Computer Architectures and Digital Signal Processing (400 level).

Selected Topics:

1. Application specific architectures for DSP applications; Systolic arrays (automated mapping procedures); data path design (fast adders, multipliers, barrel shifters); pipelining and parallel processing of filters; DSP processors
2. High level synthesis: scheduling and allocation algorithms (list-based and force-directed scheduling, ILP)
3. Low power design of digital systems: optimizations at the algorithmic and architectural level, high level synthesis for low power, low energy compilation, low power memory design, low power algorithm design
4. Parallel algorithms (sorting, FFT and some image processing kernels) and their implementation on SIMD arrays (mesh, hypercube interconnection)
5. Miscellaneous topics (memory design for embedded systems, hardware-software co-design, reconfigurable computing)

Course Information:

Text:

There is no fixed text for this course. The instructor's notes will be available in the Nobel Science Library (reserve section). The supplementary texts for this course are

1. (*)Vijay K. Madiseti, *VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis*, IEEE Press.
2. (*)S. Y. Kung, *VLSI Array Processors*, Prentice Hall.
3. (*)K. K. Parhi, *VLSI Digital Signal Processing Systems. Design and Implementation*, Wiley.
4. De Micheli, *Synthesis and Optimization of Digital Circuits*, McGraw Hill.
5. A. Chandrakasan and R. Brodersen, *Low Power Digital CMOS Design*, Kluwer Academic Publishers.
6. (*)A. Raghunathan, N. K. Jha and S. Dey, *High-Level Power Analysis and Optimization*, Kluwer Academic Publishers.
7. (*)F. T. Leighton, *Introduction to Parallel Algorithms and Architectures: Arrays, Trees, Hypercubes*, Morgan Kaufman.

Grading: 5-6 homework assignments, 1 term/research paper, 2 midterm exams and 1 comprehensive final exam.

Grading policy: Exam 1: 20%, Exam 2: 20%, Final 30%, Term paper: 20%, Homework assignments: 10%.

Other information:

Exam 1 will be held on 16th October, Exam 2 will be held on 20th November, and the final exam will be held on 15th December.