

An Efficient Control Point Insertion Technique for Leakage Reduction of Scaled CMOS Circuits

H. Rahman, *Student Member, IEEE*, and C. Chakrabarti, *Senior Member, IEEE*

Abstract—Leakage power reduction is extremely important in the design of scaled CMOS logic circuits. The dominant leakage components of such circuits are the subthreshold leakage and the thin-oxide gate leakage. This paper describes an efficient leakage reduction method that considers both these components, and is based on the selective insertion of control points. The selection is based on the leakage reduction potential and the delay insensitivity of the candidate gates. Simulations on the ISCAS85 benchmark circuits show that this method results in ~67% leakage reduction with no speed degradation when control points are added to 93% of the gates compared to the leakage of the baseline circuit whose inputs have been subjected to the minimum leakage vector.

Index Terms—Leakage current reduction, control point insertion, MLV, leakage sensitivity, low power design.

I. INTRODUCTION

Technology scaling enables us to integrate huge number of transistors on chip for higher performance. This comes at the price of increase in both static and dynamic power consumption. It is predicted that the leakage will increase 7.5 fold and the total power consumption will increase five fold for every new microprocessor-chip generation [1]. Thus for scaled technologies, leakage power reduction is an essential design component.

There are different mechanisms that contribute to leakage power. These include subthreshold leakage, thin-oxide gate leakage, band-to-band-tunneling (BTBT) leakage, etc. [2]. The existing work on leakage power reduction is aimed at reducing the subthreshold component of leakage. These include techniques based on- 1) identifying and employing the minimum leakage vector (MLV) [3][4], and control point insertion on the MLV circuit to reduce leakage further [4], 2) introducing multiple threshold voltage CMOS (MTCMOS) for a cluster of transistors to gate the power supply OFF [5], 3) using dual V_{th} to balance performance and leakage reduction [6], and 4) inserting transistors in a stack to reduce leakage [7]. However, with technology scaling especially when gate oxide thickness is less than 20Å, thin-oxide gate leakage is an

important component of the total leakage power. A transistor-level technique to reduce leakage, including thin-oxide gate leakage, was proposed in [8]. This technique uses pin re-ordering to reduce the gate oxide leakage. Another technique for gate leakage reduction that was recently proposed uses efficient transistor stacking [9].

This paper describes an efficient technique to reduce the leakage power (subthreshold and thin-oxide gate leakage) in CMOS circuits. The method is based on gate level restructuring and selective insertion of control points. The control points are selected based on their leakage reduction potential. The main contributions are-

1) Development of a heuristic algorithm for control point insertion that maximizes leakage reduction when *delay is not a constraint*. Simulation results on ISCAS85 benchmarks show that the average leakage reduction is ~25% when control points are added to 20% of the gates, compared to the baseline circuit whose inputs are the minimum leakage vector.

2) Development of a heuristic algorithm for control point insertion that maximizes leakage reduction *given a delay constraint*. For ISCAS85 benchmark circuits, control points can be added to about 93% of gates without any speed degradation resulting in an average leakage reduction of ~67%.

3) Development of an efficient algorithm that select the gates from a pre-select group of gates for control point insertion. This algorithm has comparable performance, considers only a subset of candidate gates and is considerably faster.

The rest of the paper is organized as follows: Section II introduces the control point insertion based technique for leakage power reduction. Section III shows the simulation results for the proposed leakage reduction methods. Section IV concludes the paper.

II. LEAKAGE CONTROL USING CONTROL POINT INSERTION

The leakage power consumption during the standby mode can be significantly reduced if the inputs to the circuit are chosen carefully. Table I describes the leakage of a three input NAND gate for different input combinations for a technology with feature size 65nm and 17Å gate oxide thickness. The leakage corresponding to input vector ‘100’ is 16 times smaller than that corresponding to vector ‘111’. Thus choosing the input corresponding to minimum leakage (referred to in the literature as the minimum leakage vector (MLV)) is the first

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