A MEMS-Based Power-Scalable Hearing Aid Analog Front End

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Abstract—A dual-channel directional digital hearing aid front end using microelectromechanical-systems microphones, and an adaptive-power analog processing signal chain are presented. The analog front end consists of a double differential amplifier-based capacitance-to-voltage conversion circuit, 40-dB variable gain amplifier (VGA) and a power-scalable continuous time sigma delta analog-to-digital converter (ADC), with 68-dB signal-to-noise ratio dissipating 67 μW from a 1.2-V supply. The MEMS microphones are fabricated using a standard surface micromachining technology. The VGA and power-scalable ADC are fabricated on a 0.25-μm complementary metal–oxide semiconductor TSMC process.

Index Terms—Continuous time sigma-delta modulation, digital hearing aids, directional microphone array, microelectromechanical-systems (MEMS) microphone.

I. INTRODUCTION

HEARING loss is one of the most common human impairments. It is estimated that by year 2015 more than 700 million people will suffer mild deafness [1]. Most can be helped by hearing aid devices depending on the severity of their hearing loss.

This paper describes the implementation and characterization details of a dual channel transmitter front end (TFE) for digital hearing aid (DHA) applications that use novel microelectromechanical-systems (MEMS) audio transducers and ultra-low power-scalable analog-to-digital converters (ADCs), which enable a very low form factor, energy-efficient implementation for next-generation DHA. The contribution of the design is the implementation of the dual channel MEMS microphones and power-scalable \( \Sigma \Delta \) ADC system.

The first generation of hearing aids usually consisted of analog variable gain amplifiers, electret microphones and speakers that compensated for hearing loss. They dissipated a considerable amount of power and had flat frequency characteristics that made these devices uncomfortable for most patients since hearing loss usually varies across different frequencies [1]. The next generation of devices adopted analog filter banks in which band-pass filters were used in parallel to amplify the acoustic signal to a specific level in each different frequency band. This design, however, resulted in bulky devices that still required high power consumption [2]. A major breakthrough was achieved through the development of DHAs that exploited the power of digital signal processors (DSPs) that allowed full programmability and customization to a patient’s hearing characteristic [3]–[7].

A typical DHA system, shown in Fig. 1, consists of a Transmitter Front-End (TFE), DSP, and a Receiver Front-End (RFE). The TFE consists of the microphone, a variable gain amplifier (VGA) and an ADC. The RFE receives the processed digital signal from the DSP and converts it to the analog domain. At the backend, a speaker delivers the acoustic sound to excite the patient’s eardrums.

One of the major issues with existing DHAs is the rapid degradation of performance in noisy environments in which the TFE becomes saturated due to the ambient acoustic content and background noise. Background noise interferes with the desired conversation thereby impairing intelligibility. While the use of a very high dynamic range TFE can help relieving this problem, it comes at the expense of high power consumption and complexity.

Recently developed DHAs also employ microphone arrays combined with adaptive array processing that improve audio quality and perception in real-life environments through noise cancellation mechanisms. Directional DHAs exploit the use of multiple microphone arrays (MMAs) to provide the patient with information on the spatial position of the desired acoustic source, while attenuating the ambient noise at the same time [8]. MMAs apply adaptive beam forming techniques to estimate the signal direction and cancel ambient noise [9], [10].

MMAs’ microphone characteristics and performance are important features of modern DHA devices. The most widely used microphones in hearing aids are electret microphones; however their large size prohibits the application of MMA techniques in completely in-the-ear-canal systems.

MMA hearing systems require precise adaptive matching of the gain and phase responses of both of the audio transducers and the analog front ends of each channel. For example, to achieve 10 dB of background noise cancellation, the gain of the two transmitter front ends should match within or less than 0.5 dB [8]. This implementation enables a MMA hearing system
with small size due to high level of integration and low mismatch in the amplification gains of the two channels. A small size dual-channel approach allows using two microphones per ear, giving directionality information to the patient.

The paper is organized as follows: Section II describes the motivations behind the choice of an adaptive signal-to-noise ratio (SNR) hearing aid architecture and then provides system specifications. Section III provides details of the implemented MEMS microphone and electrical interface. Section IV presents the front-end adaptive modulator design and implementation. Section V describes the physical IC design and measurement data. Finally, Section VI provides a conclusion along with a summary of the research.

II. ADAPTIVE HEARING AID

In general, the dynamic range and power level of an audio signal have different characteristics in different environments. As illustrated in Fig. 2(a), the audio spectrum of a conversation in quiet environments shows that the noise floor is at about 0 dB-SPL (dB Sound Pressure Level), and the acoustic signal has a 65-dB dynamic range. Fig. 2(b) shows the spectrum of the same conversation in a noisy environment (i.e., street) where the noise floor has increased to 25 dB-SPL and the dynamic range is now only 55 dB. Clearly, to cope with the ambient noise, the person who is speaking raises his voice level, but only up to a certain level. Consequently, it is clear that changes in signal power, dynamic range and noise floor can all be exploited to optimize the TFE circuit power consumption. In fact, in high background noise environments, the DHA system can decide to relax the front-end noise performance and optimize its parameters to avoid degradation (i.e., clipping) of the high sound-level desired signal.

Conventional hearing aid architectures have a fixed front-end dynamic range (e.g., as high as 120 dB) to cope with different ambient noise conditions but require high power consumption. In contrast, the proposed architecture adapts to noise floor conditions by adjusting system linearity and SNR of the analog front end (AFE) to maintain optimal performance. This architecture can optimize power consumption depending on the ambient conditions, thereby maximizing battery life. However, changing the system architecture to scale SNR can lead to transient artifacts, such as clicks or pops, or potential system instability. These issues have been also addressed in this work.

The target requirements of a hearing aid are summarized in Table I, and the implemented DHA architecture is shown in Fig. 3. In Fig. 3, incident acoustic waves on the dual MEMS microphones are converted into capacitive modulations. A microphone interface circuit (i.e., C2V in Fig. 3) translates the capacitive modulation into an electrical signal. A VGA is employed...
to set the optimal voltage level for the following ADC stage. An adaptive dynamic range fourth-order continuous time ΣΔ modulator is employed as the ADC. Ambient noise reduction and directivity are achieved through manipulation of the phase information of the two incoming channels in the back-end DSP and are adjusted to each individual patient’s hearing needs.

This system implements power/SNR scalability at the TFE to maximize battery life and optimize noise performance. Furthermore, in the following sections it will be shown how the adopted scaling technique avoids transient noise glitches in the RFE, which can lead to user’s ear fatigue and hearing discomfort.

III. MEMS MICROPHONE AND INTERFACE

A. Capacitive MEMS Microphone System

Fig. 4 depicts the construction of the capacitive MEMS microphone. The device size is 2.5 × 2.5 × 0.5 mm³ and it consists of a multi layered parylene diaphragm suspended over a silicon substrate [11]–[13]. The 1 μm gap between the diaphragm and substrate forms a parallel plate capacitor. The substrate acts as the capacitor backplate and acoustic holes are etched from the backside of the substrate to let the air in the gap move freely.

Minute capacitance variations of tens of femto farads, generated by the MEMS microphone is then converted into an electrical signal by a capacitive interface circuit. The design of the interface presents unique challenges due to the small sensing capacitance, the high output impedance, robust dc bias requirements, and circuit noise (mechanical and electrical).

A typical MEMS condenser microphone needs to be connected to a bias voltage source through a high impedance path [14]. To first order, the MEMS microphone can be modeled as a variable capacitor. Sound pressure moves one side of the parallel plate capacitor, creating a capacitance change. The charge $Q(t)$ vs. voltage $V(t)$ relationship of a capacitor $C_{MIC}(t)$ is expressed by

$$Q(t) = C_{MIC}(t) \cdot V(t).$$

(1)

The sensed voltage of a MEMS microphone can be derived from (1), by applying the charge conservation law

$$V_{SENSE} = \frac{\Delta C}{C_{MIC,DC}} \cdot V_{Bias}$$

(2)

where $\Delta C$ is the capacitance variation, $C_{MIC,DC}$ is the dc capacitance value and $V_{Bias}$ is the dc bias voltage of the microphone.

Fig. 5 shows the measured capacitance change as the dc voltage bias is swept from 100 mV to 900 mV. When the dc bias voltage is in the 700–900 mV range, the capacitance change of the microphone peaks and saturates around 100 fF. The 200 fF data point is an outlier in Fig. 5.

The capacitance change is converted to voltage signal by a capacitance-voltage interface, which will be discussed in section C. Fig. 6 shows the acoustic response of the MEMS microphone. A 1 kHz acoustic signal with 20 to 80 dB SPL was applied to the MEMS microphone. The measured MEMS microphone’s capacitance modulation shows a linear characteristic.

B. MEMS Microphone Interface

Capacitive sensing circuit architectures can be roughly divided into three broad categories: 1) the switched capacitor charge integration (SCI) usually implemented in CMOS, with
An ideal FDDA with infinite forward gain \(A\) in negative feedback configuration forces the following relationship between the two differential inputs

\[
u_{\text{PP}} - \nu_{\text{PN}} = \nu_{\text{AP}} - \nu_{\text{AN}}\text{*} \tag{3}\]

Since there are two differential pairs, the gain matching of the two parallel transconductance stages (i.e., \(g_{m1}\) and \(g_{m2}\)) is an important issue and sufficient matching to guarantee correct circuit operation is required. The signal transfer function of the FDDA can be written as

\[
u_{\text{OD}} = A_d \cdot \left[\left(\nu_{\text{D}} - |\nu_{\text{diff}}|\right) + \frac{1}{\text{CMMR}_P} \cdot (\nu_{\text{CP}} - \nu_{\text{CPD}}) + \frac{1}{\text{CMMR}_A} \cdot (\nu_{\text{CA}} - \nu_{\text{CAM})} + \frac{1}{\text{CMMR}_d} \cdot (\nu_{\text{CD}} - \nu_{\text{CDO}}]\right) \tag{4}\]

where \(A_d\) and \(\nu_{\text{diff}}\) are the differential gain and input-referred offset, defined similar to the case of conventional opamps. However, the \(\text{CMMR}_P, \text{CMMR}_A\) parameters are unique to the FDDA due to the dual input pairs. The \(\text{CMMR}_P\) and \(\text{CMMR}_A\) are the common mode rejection ratios of the primary and the auxiliary input pairs, whereas the \(\text{CMMR}_d\) is a measure of the difference of the differential inputs, which also becomes a common mode signal, defined as

\[
\text{CMRR}_d \approx \frac{1}{\frac{sw}{gm2}} \tag{6}\]

where \(\frac{sw}{gm2}\) is a measure of the difference of the differential inputs.

Fig. 8 shows the device level schematic of the FDDA. The input pairs of the FDDA are implemented using PMOS devices with large gate areas in order to reduce the flicker noise contribution. The output consists of a class AB stage to drive the relatively low input impedance of the next stage. The FDDA has a dc gain of 75 dB, and GBW of 9 MHz.

C. MEMS Capacitive Readout Linearity

The interface circuit is expected to achieve more than 90 dB dynamic range as shown in Fig. 10. A plot of the simulated THD as a function of the input sound pressure in dBSPL at 1.05 kHz is shown in Fig. 11. No significant distortion is manifested in the front and the THD is less than 1% (−40 dB) for a SPL less than 100 dB.
Fig. 10. Dynamic range simulation results.

Fig. 11. THD of the differential output voltage Vs SPL at 1.05 kHz.

D. VGA Design

A VGA is used to amplify the signal in order to maximize the resolution of the following ΔΣ ADC at various input signal levels. The VGA, shown in Fig. 7, includes a linearized MOS resistor at the input and an OTA with resistive feedback [23], [24]. The input resistor is a cross-coupled depletion-mode NMOS transistor pair, whereas the feedback resistor is a high-resistive programmable poly resistor with four settings of 100, 200, 400, and 800 kΩ. The gate voltage of the cross-coupled transistors sets the gain of the VGA together with the switchable feedback resistor banks. The simulation results of the VGA programmable gain are reported in Fig. 12. The schematic of the OTA used in the VGA is shown in Fig. 13. A cross-coupled NMOS load is used to increase the gain with positive feedback, which is then followed by a class-B output stage. The class-B stage increases the output current drive capability while keeping the quiescent current at an optimum value to reduce power consumption.

IV. FRONT-END ARCHITECTURE AND CIRCUIT

Fig. 14 shows the block diagram of the implemented ΔΣ architecture, which is a fourth-order continuous time ΔΣ modulator with a 1.5-b quantizer (−1, 0, 1) [25]. The input stage is an active-RC integrator whereas the subsequent stages are gm-C integrators. Furthermore, the topology uses return-to-zero current-steering DACs in the feedback while two comparators implement the 1.5-b flash quantizer.

The design of ΔΣ ADCs for the DHA architectures is very challenging because of the requirements for extremely low power consumption and high SNR at the same time. In discrete-time ΔΣ modulators, integrators are usually implemented using switched capacitor circuit techniques. However,
in order to satisfy the SNR requirement, the switched-capacitor integrators are required to settle to their final value in half the clock period which, in turn, requires a very high gain bandwidth product (GBW) for the OTAs and, thus, high-power consumption. In contrast, the loop filter frequency response of continuous time modulators is required to cover only the signal bandwidth, which usually results in a much lower GBW product requirement and then power consumption [26].

A. Design of the $\Sigma\Delta$ Loop

To simplify the ADC system design, a discrete-time prototype for the $\Sigma\Delta$ loop was used as a starting point and then converted to a continuous time equivalent system by using impulse invariant transform [25], [28]. The resulting $\Sigma\Delta$ loop is a fourth-order modulator with an in-band optimized zero in the noise transfer function (NTF). The simulated NTF and signal transfer functions (STF) of the designed discrete time prototype are shown in Fig. 15.

The block diagram shown in Fig. 16 was used to validate the discrete-to-continuous time transformation. Lossy integrator models were used to derive each integrator’s dc gain specification to achieve the required SQNR (signal-to-quantization-noise ratio). A minimum dc gain of 60 dB in the first integrator OTA is needed to achieve the desired SQNR level.

B. First-Stage Adaptive Active RCI Integrator

Power scaling of the system is implemented at the first integrator stage of the $\Sigma\Delta$ modulator wherein the highest power consumption is budgeted to the first stage in order to guarantee high SNR and linearity. Three parallel binary-scaled OTAs implement the power/SNR scaling, which consists of 4 power consumption steps (i.e., 8.4, 16.8, 33.6, and 67.2 $\mu$W, respectively, from a 1.2-V supply). Fig. 17 shows the schematic of the unit OTA used to build the adaptive active RC integrator. Depending on which OTAs are enabled, the input integration resistors are scaled accordingly to increase the linearity performance (Fig. 19). At low power levels and high input sound levels, higher input resistance is used to decrease the integration current thereby optimizing the linearity and dynamic range of the first stage at the expense of higher input-referred noise. However, as discussed in Section II, in this situation, ambient noise dominates the system noise budget and, therefore, the noise performance of the ADC can be relaxed.

In order to maintain a constant loop filter response, integration capacitors are scaled as well when the input resistor is varied. The input resistor is scaled to 100, 200, 400, and 800 k$\Omega$ when lowering the power consumption while the integration capacitor can assume the values of 100, 50, 25, and 12.5 pF, respectively. Furthermore, additional fine-tuning of resistors and capacitors is employed to guarantee loop frequency response accuracy against process variations and mismatches.

Fig. 18 shows the simulated input-referred noise spectrum of the active-RC integrator when different parallel OTAs are enabled (i.e., at different levels of power/SNR scaling of the integrator performance).

The calculated integrated input-referred noise in a 10-KHz bandwidth and corresponding SNR value are shown in Table I. Effective SNR of the system can be varied from 81 to 90 dB with the appropriate power setting.

C. Switching Transients

Discrete SD modulators usually exploit idle clock phases to perform architecture reconfigurations without affecting the signal integrity (i.e., glitches, bursts). However, there is no available clock phase to change the power/SNR configuration of the first integrator in the adopted continuous time modulator. Thus, in order to avoid hearable signal artifacts (e.g., popping sounds) and also modulator instability, the transient response
of the system must be carefully analyzed when parallel OTAs are engaged and/or disengaged.

Ideally, when the auxiliary OTAs are connected, instability and glitches will be avoided as long as the input and output voltages of the auxiliary OTA settle to the same values of the OTA already active in the loop. Unfortunately, this is not feasible because the input signal and the feedback DAC (DAC1) continuously change the input and output node voltages of the first integrator so that a very fast tracking of the input and the output of the integrator would be required, which would lead to high power and die area costs.

However, a system analysis shows that if the input and the output of the auxiliary integrator are kept at the common mode voltage before insertion, the effects of the transient are reduced and the impact to the output of the modulator is negligible. The simplified schematic of the active-RC integrator with two parallel OTAs is shown in Fig. 19. Before connecting the additional OTA into the loop, its input nodes are connected to the common mode voltage $V_{CM}$, while the feedback capacitor is shorted by transmission-gate (TG) switches, so that the OTA is placed into a unity gain configuration with zero differential input. After the additional OTA is powered up and its output nodes are settled to the common mode voltage, the input nodes are disconnected from the common mode supply, and the TG switches that are shorting the feedback capacitors are opened. The input resistors are then scaled to the required value only after the input and output nodes of the additional OTA are connected to the whole integrator. This power up procedure ensures that the transient effect to the $\Sigma\Delta$ loop is negligible.

When the auxiliary OTAs disengage, the effect on the loop stability is inherently very small. Indeed, the extra integration capacitance is disconnected from the loop and the integration resistor size is increased accordingly. Since the capacitors are already precharged from the previous operation, the only disturbance is due to charge injection from the CMOS switches, which has been minimized by adopting well known techniques [29].

Adaptive power scaling of the fourth-order CT $\Sigma\Delta$ achieves 68-dB SNR at 120 $\mu$W, which can be scaled down to 61-dB SNR with 67 $\mu$W power consumption. Fig. 20 shows measured noise level with zero input for the four power settings. The noise floor decreases about 2–3 dB with each doubling of the first integrator power. Fig. 21 shows the transient response of the power switching. In this test the power of the modulator is changed from minimum to maximum and vice-versa every 1 ms. The digital bit stream is decimated and filtered with a seventh-order digital Butterworth filter. The output does not show dramatic artifacts (popping or clicking). This measurement shows that
when the environment conditions change and the DSP commands a different power level setting, the modulator adapts to the change quickly, with only very little effect on the signal amplitude. However, environment changes happen at a low repetition rate in real life (e.g., once every few seconds or minutes). Therefore the amplitude changes in the output will not be recognized by the user.

**D. \( g_{\text{m}} \)-C Integrators**

The \( g_{\text{m}} \) stage circuit topology that has been used as the voltage to current converter is shown in Fig. 22. A folded-cascode structure is used to maximize the integrator dc gain. Resistive source degeneration is used to set the transconductance value and improve linearity. Two helper amplifiers \( (Av) \) increase the precision of the input source followers, allowing voltages \( V_{\text{lp}} \) and \( V_{\text{hp}} \) to accurately appear at the degeneration resistor nodes [27]. The input differential voltage is thus converted into a small-signal current through \( R_{\text{deg}} \), which flows at the drains of the input PMOS devices. The differential current is then applied to the folded output stage to increase output impedance and dc gain.

The \( g_{\text{m}} \)-C integrators have a 69-dB dc gain, a power dissipation of 9.6 \( \mu \)W from a 1.2-V supply, and the integration constants are 65.9, 103.9, and 596.8 kRad/s.

**E. \( g_{\text{m}} \)-Z Noise Transfer Function (NTF) Zero**

In the modulator block diagram of Fig. 14, the local feedback \( g_{\text{c}} \) block implements a zero in the NTF just at the edge of the modulator passband, which helps to increase the SQNR by \( \sim 20 \) dB [28]. Note that his NTF zero is required in order to meet the system specifications. Because of the low frequency of the NTF zero, the required \( g_{\text{m}} \) value to implement the zero is at least two orders of magnitude lower than the other \( g_{\text{m}} \) stages.

The implemented \( g_{\text{m}} \) transconductance stage is shown in Fig. 23. The circuit consists of a modified version of the folded cascode transconductance stage. To achieve a low transconductance value without increasing the size of the degeneration resistor, the signal current of the input stage is scaled down to the desired value in three current mirroring stages (i.e., 200:40:4:1). The \( g_{\text{m}} \)-C integrator has a 42 dB dc gain, with an integration constant of 500 rad/s. The power dissipation is 5.7 \( \mu \)W from a 1.2-V supply.

**F. Comparator**

The schematic of the adopted three-level (1.5 b) quantizer is shown in Fig. 24. Return-to-Zero phase consists of a third level in the DAC. By using a three-level quantizer, the zero state is generated as a digital code, which helps the loop stability and increases the SQNR. The adopted comparator architecture consists of a preamplifier and a regenerative latch [30]. The preamplifier compares the input differential signal with the differential reference voltage. When the digital clock signal is low, the regenerative latch is equalized, and the input signal is compared; when the clock is high, the current differential at the output of the preamplifier stage triggers the regenerative latch to its final value.

As shown in Fig. 25, the quantizer uses a two-phase clock. When \( \phi_1 \) is low, the quantizer is equalized; when \( \phi_1 \) is high,
the output of the quantizer is latched. Furthermore, when \( \phi_2 \) is high, a logic AND between the output of the quantizer and the clock is performed, which gives the Return-to-Zero state. A non-overlapping clock generation circuit is used to produce the clock signals. The input to this circuit is a 50% duty-cycle clock, and the output is a clock with a larger duty cycle, which is determined by the delay of the feedback signals at NAND gates’ inputs. The current-starved delay architecture is used to guarantee that the rising edge of the clock (\( \phi_1 \)) comes later than the rising edge of the comparator enable signal (\( \phi_2 \)) [31].

G. Digital-to-Analog Converter (DAC)

Current steering non-return-to-zero (NRZ) or return-to-zero (RZ) DACs are typically used in \( \Sigma \Delta \) modulators because they enable simple feedback architecture. A complementary current source and sink architecture is used in this design to ease requirements on the common mode feedback circuit of the OTAs [32]. When a positive pulse comes from the comparator, DACs’ PMOS current sources supply a positive current to the positive integration node and NMOS current sources sink a negative current from negative integration node. With a negative pulse, direction of the current sources is inverted with PMOS current sources supplying to the negative integration node, and NMOS sources sinking current from positive integration node. For the RZ phase, the PMOS current sources are directly connected to the NMOS current sources.

The DAC1 block, shown in Fig. 26, has the most stringent requirements because it is directly applied to the modulator input nodes. In particular, DAC1 should be as linear as the whole system. Dynamic current calibration and glitch optimization is used to overcome DAC1’s non-idealities [33]. Moreover, current scaling is implemented for power/SNR optimization. A bias circuit generates gate voltages for the NMOS and PMOS current sources in the circuit. However, when the current sources are scaled up to generate the required DAC output, the NMOS and PMOS transistors are scaled differently, leading to a current mismatch. To equate the source and sink currents dynamic calibration is therefore required. During the calibration phase, the switches controlled by \( V_{zp} \) are closed. The up current \( I_{up} \) and the down current \( I_{dn} \) are equalized while all the \( V_{zp} \) switches closed. The equalization is implemented by forcing a voltage \( V_{gs} \) on the hold capacitor to compensate for the mismatch in the up PMOS and down NMOS devices. During normal DAC operation, \( V_{zp} \) switch is open and the capacitor holds the calibrated gate voltage. Usually, in a conventional dynamic calibration DAC, two identical DACs are designed [33]. During one clock phase, one of the DACs is calibrated and then during the next phase, the calibrated DAC is used in the feedback. Meanwhile, the other DAC is calibrated. The major difference between this implementation and previous DACs is that the calibration is done during the return-to-zero phase. By using this scheme, an extra DAC is not needed, which saves power and die area.

DAC2, DAC3, and DAC4 requirements are more relaxed than DAC1 because the gain of each preceding integrator stage reduces the impact of the corresponding DAC’s limitations [26]. Fig. 27 shows the implemented unity current cell of these DACs. Dynamic current calibration is not used in this case; however, a diode-based common-mode hold circuit is used to avoid the DAC common-mode drift. During the zero phase, the PMOS current source and the NMOS current source are connected to each other and because of the mismatches between the current sources with their inherent high output impedance; the output can drift either to \( V_{dd} \) or \( V_{ss} \). The diode divider sets this common mode to a known voltage in less than half of a clock period so that neither of the current sources is pushed out of saturation. This scheme reduces transient glitches, thereby improving modulator stability and the overall SQNR of the modulator.

H. Excess Loop Delay and Jitter

Fig. 28 shows a general discrete time \( \Sigma \Delta \) modulator and its continuous time counterpart [34]. The discrete time modulator and continuous time modulator are assumed equivalent if the error signal \( e[n] \) in both modulators is equivalent. In the signal
Fig. 27. Implemented DAC2, DAC3, DCA4.

Fig. 28. Excess loop delay.

Fig. 29. Jitter timing.

In the NRZ case, the feedback signal is turned on and off with the comparator output. Because of the finite turn on time, $T_3$, and the finite turn off time, $T_4$, actual current pulses are delayed from the comparator output. As a result of this delay, the next sampling occurs before the full charge transfer, resulting in excess loop delay. This characteristic leads to SNR degradation and higher signal distortion.

The effect of jitter in continuous-time SD modulators has been previously studied [35]. The effect of a clock jitter is an increase in the noise floor and then a reduction of the dynamic range of the modulator. In a higher order $\Sigma\Delta$ modulator, comparator input is de-correlated from signal amplitude. As a result of this, the jitter effect of the quantizer is negligible. On the other hand, jitter in the feedback DAC has major effects on modulator performance [35]. Because the DAC current is fed back to the integrators during a clock phase, uncertainty of the turn on and turn off time of the current sources has a major effect on system performance. Fig. 30 shows the simulated SNR degradation due to jitter on the designed fourth-order $\Sigma\Delta$ modulator. Effect on the system performance is negligible if the clock jitter is lower than 10 pS.

V. IC DESIGN AND MEASUREMENTS

Fig. 31 shows the implemented DHA system. The analog frontend is fabricated on a 0.25-μm CMOS process whereas the MEMS microphones are fabricated at the Arizona State University’s cleanroom facility with a custom MEMS process. The CT-$\Sigma\Delta$ modulator has a sampling frequency of 1 MHz; with an input signal bandwidth of 10 KHz. Fig. 32 shows the measured $\Sigma\Delta$ modulator SNR against input amplitude. At
the highest quiescent power setting, the CT $\Sigma\Delta$ modulator achieves 68-dB SNR, 65-dB SNDR, and 60-dB THD, respectively. Fig. 33 shows the measured signal transfer function of the $\Sigma\Delta$ modulator. The measured frequency response is flat over the 10-kHz bandwidth, and does not show any frequency peaking. The directivity index (DI) is defined by the ratio of radiated sound intensity at a remote point on the principal axis of a loudspeaker or other transducer, to the average intensity of the sound transmitted through a sphere passing through the remote point and concentric with the transducer. A higher directivity index proves better phase and amplitude matching between the audio signal chains. As shown in the Fig. 34 after the gain calibration is performed, overall system achieves a directivity index of 5 at 1 kHz, which provides excellent rejection of sideband audio components.
VI. CONCLUSION

In this paper, a dual-channel, power-scalable transmitter front-end digital hearing aid is presented. The system can be integrated in a multichip module, which will reduce the costs of hearing aids while offering superior battery life and background noise suppression. The MEMS microphone achieves a sensitivity of 5.2 mV/Pa with 600-mV bias. Finally, the power scalable $\Sigma\Delta$ modulator shows a 68-dB SNR over a 10-kHz bandwidth.

REFERENCES


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