

## Education

- **PhD in Computer Science and Engineering** August 2003-November 2009  
*Arizona State University, Tempe, Arizona, USA* GPA: 3.89/4.0
- **Bachelor of Engineering in Computer Science and Engineering** August 1999-June 2003  
*Jadavpur University, Jadavpur, Kolkata, INDIA* GPA: 3.78/4.0

## Relevant Courses

- *Graduate Level:* Theory of Computation, Distributed & Multiprocessor Operating Systems, Distributed Database Systems, Randomization & Approximation Algorithms, Hardware Design Languages, Electronic Design Automation, Combinatorial Algorithms and Intractability, Numerical Optimization, VLSI Architecture, Real Time Embedded Systems, Hardware-Software Codesign, Advanced Computer Networks, Computer Architecture, Operating Systems Internals.
- *Undergraduate Level:* Operating Systems, Data Structures, Design and Analysis of Algorithms, Computer Networks, Database Management Systems, Formal Language and Automata Theory, Digital Logic, Digital Circuits.

## Technical Knowledge

- Platforms: Windows 9x, Windows XP, Windows NT, Linux/Unix, Mac OS X, Solaris, VxWorks.
- Programming Skills: C, C++, Pascal, Prolog, Java, 8085 & 8086 Assembly Language, UNIX Shell programming, Perl, Verilog, SystemC, MATLAB, MPI.
- Tools and Products: gcc, VC++, VB, Cadence Circuit Simulator, Cadence VerilogXL Simulator, Synopsys Logic Synthesis tool, Celoxica and Xilinx EDA tools, Intel IXP 2400, ILOG CPLEX Optimization platform, ILOG CPLEX Concert Technology, glpsol LP solver tool, WindRiver Tornado, Version controlling systems - CVS, Subversion.
- Network Programming: Socket & Client/server (TCP/IP) programming.
- Web Programming: HTML, XHTML, CSS, HTML DOM, DHTML, XML, PHP, MySQL, JavaScript.

## Work Experience

- **Post-doctoral Research Associate** November 09 - Current  
*Computer Sc. and Engg. Dept., ASU, AZ.*
  - Identifying research problems in System-on-Chip (SoC) and Network-on-Chip (NoC) domain, Designing efficient solution techniques
  - Research in airborne networks - coverage and connectivity problems

- Teaching Associate/Research Associate** August 07 - November 09

  - *Computer Sc. and Engg. Dept., ASU, AZ.*
    - CSE355 - Introduction to Theoretical Computer Science in Fall 2007 and Fall 2009
    - CSE450 - Design and Analysis of Algorithms in Spring 2008 and Fall 2008
    - CSE550 - Combinatorial Algorithms and Intractability in Fall 2008
    - CSE430 - Operating Systems Concepts in Spring 2009
    - CSE591 - Introduction to Game Theory with Application to Networks in Spring 2009
- Internship** May 05- August 07

  - *Intel Corporation*
    - Graduate Intern in the Performance Modeling team of the Infrastructure Processor Division(IPD), currently ECPD
    - Development of Integrated Performance Modeling and Functional Modeling tool for several memory sub-units, chipsets, etc.
    - Generation of Synthetic traffic for validation of the models.
    - Publishing results for sets of experiments.
    - Study of micro-architectures for several sub-units and discussion with Architects and Software developers for possible performance bottlenecks (extensive teamwork).
- Research Associate** August 04 - May 05

  - *Computer Sc. and Engg. Dept., ASU, AZ.*
    - Developing co-design framework starting with system level specification of Network Processing Unit with real-time performance constraints.
    - Periodic submission of report and experimental results showing the progress.
- Teaching Associate** August 03 - May 04

  - *Computer Sc. and Engg. Dept., ASU, AZ.*
    - CSE355 - Introduction to Theoretical Computer Science in Fall 2003
    - CSE450 - Design and Analysis of Algorithms in Fall 2003
    - CSE340 - Principles of Programming Languages in Spring 2004

## Research Interest

My research interests include several issues in the System-on-Chip (SoC) and Network-on-Chip (NoC) domains - specifically performance and energy optimization problems, design of analytical models, mapping, scheduling and routing, etc., HW/SW codesign and Electronic Design Automation of VLSI circuits, Computational complexity of problems and development of efficient algorithms, Optimization problems in Electric Power Network systems, Airborne and Sensor Networks.

## Publications

- “Resource Mapping and Scheduling for Heterogeneous Network Processor Systems”- In Proceedings of the 2005 ACM Symposium on Architectures for Networking and Communications Systems (ANCS).
- “A New Min-Cut Problem with Application to Electrical Power Network Partitioning” - In Proceedings of the 44th Annual Allerton Conference on Communication, Control and Computing, 2006.

- Extension of the work “A New Min-Cut Problem with Application to Electrical Power Network Partitioning” - Published in European Transactions on Electrical Power, vol. 19, 2009, pp. 778-797 (published online on March 11th, 2008)
- “Energy Minimization using a Greedy Randomized Heuristic for the Voltage Assignment Problem in NoC” - In Proceedings of the 21st IEEE International SOC Conference (SOCC), 2008.
- “Energy Efficient Application Mapping to NoC Processing Elements Operating at Multiple Voltage Levels” - In Proceedings of the 3rd ACM/IEEE International Symposium on Networks-on-Chip (NOCS), 2009.
- “A Unified Approach for Multiple Multicast Tree Construction and Max-Min Fair Rate Allocation” - In Proceedings of 2009 IEEE International Workshop on High Performance Switching and Routing (HPSR).
- “Avoiding Hotspot Formation of Sensor Networks for Temperature Sensitive Environments” - In Proceedings of the 2009 IEEE Globecom conference.
- “Impact of Region-based Faults on the Connectivity of Wireless Networks” - In Proceedings of 47th Annual Allerton Conference on Communication, Control and Computing, 2009.
- “Efficient Mapping and Voltage Islanding Technique for Energy Minimization in NoC under Design Constraints” - In Proceedings of 2010 ACM Symposium on Applied Computing (ACM SAC) - Embedded Systems Track.
- “Power Efficient Voltage Islanding for Systems-on-Chip from a Floorplanning Perspective” - In Proceedings of the Conference on Design, Automation and Test in Europe (DATE), 2010.
- “Energy Efficient Mapping and Voltage Islanding for Regular NoC under Design Constraints” - accepted for publication in the International Journal of High Performance System Architecture (special issue on Power-efficient, High Performance General Purpose and Application Specific Computing Architectures).
- “An Analytical Framework with Bounded Deflection Adaptive Routing for Networks-on-Chip” - In Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2010.
- “Energy Efficient Application Mapping to NoC Processing Elements with Voltage Islanding under Performance Constraints” - in preparation for submission to the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.
- “Connectivity, Coverage and Routing for an Airborne Network” - submitted to the AIAA Journal of Aerospace Computing, Information and Communication.
- “Beyond Connectivity - New Metrics to Evaluate Robustness of Networks” - submitted to 30th IEEE International Conference on Computer Communications (Infocom 2011).

## Projects

- **Arizona State University (Related to Coursework)**
  - Client Server system using distributed shared memory on UNIX platform.
  - Implementation of certain functionalities of a generic Network Processor at the RTL level using Verilog (teamwork).
  - Implementation of heuristic algorithms for VLSI physical design (Partitioning, Placement).

- System level design of MPEG-2 video decoder using SystemC and targeting implementation on platform FPGA (teamwork).
- Implementation of selected eCos APIs (related to conditional variables) using VxWorks system calls.
- Implementation of device driver in vxWorks for Microsoft 2.1 Plug and Play serial mouse.

- **Arizona State University (Research Project)**

- Hardware-Software Co-design of Network Processor Systems.
- Working on a co-design framework that starts with a homogeneous system-level specification for a Network Processing Unit with real-time performance constraints and produces a low-cost heterogeneous architecture that satisfies all the specified constraints.

- **Jadavpur University, India (BE Project)**

- Design and implementation of a Voice Mail system at the chip level; Intel 8085, 8086 microprocessors and 8051 microcontroller used for building up the system (teamwork).
- Design of an automated railway reservation system (front end and back end) using Visual Basic (teamwork).

## Honors

- Awarded the 2nd prize for the *Mathematical Modeling Contest* organized by Phoenix City Council in October, 2007.
- Student recipient of the *Motorola University Partnership in Research award* for the year 2004-2005.
- Awarded the 7th position in 12th grade state level examination in West Bengal, India out of 400,000 students.