

Reiley Jeyapaul

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Research Interests

- Analytical and Computational Modeling of the processor cache.
- Compiler level optimizations to eradicate Soft Error issues.
- Code transformations for energy efficient utilization of microarchitecture techniques.
- Microarchitecture and Compiler techniques for Multi Core processors.

Academics

- Jan 2009 – till present [GPA : 4.0/4.0]
Ph.D in Computer Science at Compiler and Microarchitecture Laboratory, SCIDSE, ASU
- Aug 2006 – Dec 2008
MS in Electrical Engineering, ASU [GPA : 3.6/4.0]
Thesis : Accurate Analytical Vulnerability Model for reduction of Failure due to Soft Errors.
- Sep 2000 – May 2004
BE in Electronics and Communication Engineering, India [GPA : 3.9/4.0]

Record of Skills

- Design Tools : CADENCE, Verilog, VHDL, H-SPICE, CADSTAR
- Programming : C, C++, VC++, MIPS assembly language, Perl scripting
- Simulators/Tools : SimpleScalar, HotSpot, PTScalar, Omega Library, Polylib
- Software : MATLAB, Rational (Purify, Quantify, Pure Coverage), MSVisio
- Operating System : Linux, UNIX , MS Windows (x86 and x64)

Publications

- “Code Transformations for TLB Power Reduction”, **Reiley Jeyapaul**, Aviral Shrivastava, **VLSI 2009**. [acceptance rate 26%]
- “Static Analysis to Mitigate Soft Error failures in processors”, **Reiley Jeyapaul**, Jongeun Lee and Aviral Shrivastava, Submitted for review.

Experience Summary

Graduate Research Assistant, Consortium for Embedded Systems [Sep 06 – Present]
Department of Computer Science, ASU.

Design and develop compiler level techniques and methodologies to alleviate the issues of power and reliability in today’s and future embedded processors and multi-core processor architectures.

Module Leader (Oct 05-Jul 06) || **Software Engineer** (Jun 04-Sep 05)

Larsen & Toubro Infotech Ltd, Chennai, INDIA.

[Jun 04 – Jul 06]

Designed and developed system level multi-threaded services and driver-interface applications for Win32 and Win64 OS. Worked with MS Windows API developing applications in VC++ IDE.

Relevant Coursework

Design and Analysis of Algorithms, Combinatorial Algorithms and Intractability,
Compilers for Embedded Systems, Low Power Computer-Architecture, Computer Architecture I,
Advanced VLSI Design , Semiconductor Device Theory, Introduction to Theory of Computation.

Research Projects *(at Compiler Microarchitecture Laboratory)*

CE³S: Compiler Enhanced Energy Efficient Shielding of Registers

- Through analysis and experiments, determined that the register usage pattern can be altered by the compiler and therefore a fixed order of registers can be shielded.
- Using a fixed register-order for shielding with highly vulnerability data would greatly reduce the energy overhead and also vulnerability reduction of Register File.
- Designed and implemented a compiler register reallocation algorithm to ensure highly-vulnerable and least accessed variables to specific order of registers
- The algorithm was implemented in the GCC (v2.6.3) compiler.

Code Transformation Technique to reduce TLB switching energy

- Developed a novel access-reordering code transformation technique to reduce the number of page switches in the TLB.
- Implemented the technique for a new TLB architecture (use-last) designed by Intel.
- Experimentally demonstrated the reduction in energy dissipation of processors.

Compiler Technique to mitigate failures due to Soft Errors

- Developed a compiler technique to alter the data access pattern in a program, thereby reducing the failure rate (due to soft errors), of the system.
- Analyzed various code transformations to determine their impact on vulnerability
- Implemented an analytical cache model for failure rate estimation.
- Experimentally demonstrated the impact of the transformations using SimpleScalar cycle-accurate simulator.

Academic Projects

Arizona State University, Fulton School of Engineering

[Sep 06 – May 08]

Design of Out-Of-Order Issue Queue for 4-issue processor

- Designed an energy efficient and fast issue queue using CAM arrays to store data.
- A priority encoding logic was implemented for oldest-first execution of instructions.
- The issue queue consisted of 32 entries and optimized for energy and performance

Design and Development of 4KB SRAM memory bank

- Designed a reliable 6T-SRAM memory bank to work across process corners.
- Designed all associated circuitry involved in the working of the memory bank.
- Schematic design and standard-cell layout practice for the memory bank.

Low-Power Design of a Multi-Bit Viterbi Decoder

- Designed a fast and very low power multi-bit Viterbi Decoder.
- Schematic design and simulation using CADENCE-spectre design tools.
- Optimal Standard-Cell layout was practiced to realize the circuit in minimal area.

University of Madras, SRM Engineering College

[Sep 00 – May 04]

Design and development of Microcontroller based Digital I/O Network Node

- Real time system architecture and Programming of the microcontroller using Cross-C
- Circuit design and design implementation using CADSTAR
- Testing of the circuit using Bread-board testing and then integrated board testing

References will be provided on request.