A Monolithic Three-Axis Micro-g Micromachined Silicon Capacitive Accelerometer

Junseok Chae, Member, IEEE, Haluk Kulah, Member, IEEE, and Khalil Najafi, Fellow, IEEE

Abstract—A monolithic three-axis micro-g resolution silicon capacitive accelerometer system utilizing a combined surface and bulk micromachining technology is demonstrated. The accelerometer system consists of three individual single-axis accelerometers fabricated in a single substrate using a common fabrication process. All three devices have 475-μm-thick silicon proof-mass, large area polysilicon sense/drive electrodes, and small sensing gap (<1.2 μm) formed by a sacrificial oxide layer. The fabricated accelerometer is 7 × 9 mm² in size, has 100 Hz bandwidth, >5 pF/g measured sensitivity and calculated sub-μg/√Hz mechanical noise floor for all three axes. The total measured noise floor of the hybrid accelerometer assembled with a CMOS interface circuit is 1.60 μg/√Hz (1.5 kHz) and 1.08 μg/√Hz (>600 Hz) for in-plane and out-of-plane devices, respectively.

Index Terms—Inertial sensors, micro-g, micromachined accelerometer, sigma-delta, switched-capacitor, three-axis accelerometer.

I. INTRODUCTION

MEMS (microelectromechanical systems) have attracted much attention since miniaturized mechanical structures were developed by utilizing semiconductor fabrication technology. Sensors for measuring pressure, acceleration, and devices such as the inkjet printer head have been commercialized since 1970s [1]–[3]. Among them, the micromachined pressure sensor and accelerometer have been one of the most successful commercialized MEMS products for automotive applications [4]. In addition to low-medium performance accelerometers, demand for high-performance devices aiming at inertial navigation/guidance, unmanned aerial vehicles (UAV’s), seismometry, space gravity instruments, and many consumer applications such as computer peripherals, headset for virtual reality, has constantly increased due to the potential features of low-cost, small-size, and low-power dissipation [5]–[7].

The requirements for these high-performance applications include low noise, high sensitivity, small drift, excellent stability, small off-axis sensitivity, low-temperature sensitivity, and high resolution [8], [9]. In addition, many of these applications require measurements along more than one axis. Of the requirements mentioned above, accuracy (stability) and resolution are the most challenging. The former is very dependent on the overall design and structure of the device, as well as on the packaging and mounting and the materials used. The latter, depends heavily on the design and specific features of the sensing element and its readout electronics.

Since the first micromachined accelerometer was introduced in the late 1970s [1], several accelerometers have been developed to achieve micro-g resolution. However, most of the reported high-performance capacitive accelerometers are only sensitive to a single-axis [10]–[13]. For some applications such as inertial navigation, a precision three-axis accelerometer system is highly desired. In order to build such a system, typically individual devices are hybrid mounted on the faces of a cube. This introduces misalignment of individual sensors, increases the cost, occupies large area, and requires complicated packaging [14], [15].

Although a few integrated single-chip three-axis capacitive microaccelerometers have been reported [16]–[18], due to small mass, low sensitivity, or low-performance readout circuit, their output noise floors are at best in the 0.04–1 mg/√Hz range. Our group has reported in-plane (x- and y-axis) and out-of-plane (z-axis) capacitive silicon accelerometers with micro-g resolution [19], [20]. Both implement a combined surface and bulk micromachining technology [21] and utilize an almost identical fabrication process. Thus, two in-plane and one out-of-plane accelerometers can be integrated onto a single substrate. This paper presents a fully integrated three-axis accelerometer with a hybrid low-noise CMOS readout circuit providing micro-g measurement resolution for all three axes. In the following sections, first the structure of the three-axis accelerometer is described. Next, estimated performance with interface electronics, and accelerometer fabrication are discussed. Finally, measurement results of the accelerometer-CMOS readout circuit system such as sensitivity, noise floor, temperature, and drift characteristics are presented.

II. SENSOR DESIGN

A. Accelerometer Structure

Fig. 1 shows the structure of the three-axis accelerometer. The three-axis chip is a monolithic integration of three individual single-axis accelerometers. This reduces the size of the
entire system. The lithographically defined alignment of the three single-axis devices minimizes cross-axis sensitivity due to the misalignment of individual devices. The three-axis accelerometer is mechanically connected together by polysilicon connectors, which electrically isolate the three accelerometers to ensure cross-talk free operation. Unlike surface micromachined devices, the three-axis chip utilizes a combined surface and bulk micromachining technology so that it has large structural mass (full wafer thick, 475 μm), and large area electrodes with small sensing gap (<1.5 μm), which produces high-sensitivity low-noise accelerometers. The proof-mass is defined by anisotropic wet etching at the end of fabrication. Polysilicon electrodes span the entire proof-mass and are anchored to a supporting rim.

Fig. 2 shows individual device structures. The Out-of-plane accelerometer has its proof-mass separated by a narrow air gap from a fixed conductive plate made of polysilicon located at the top and the bottom of the proof-mass, establishing a parallel plate capacitor. The polysilicon plate, while thin, is made very stiff by vertical stiffeners to ensure stable closed-loop operation [22]. In order to reduce damping to achieve sub-μg/√Hz mechanical noise, the polysilicon plate is perforated to allow the gas between the plate and the proof-mass to escape easily through the holes. According to our device structure, the damping needs to be $1.37 \times 10^{-2}$ [N · s/m] to satisfy 0.7 μg/√Hz mechanical noise density. Detail derivations and equations regarding the polysilicon plate perforation to achieve very low mechanical noise are presented in [23]. The in-plane accelerometer has its proof-mass supported using high aspect-ratio polysilicon springs, which are formed by refilling deep-etched trenches. Polysilicon trench refilling is also used to form vertical sense/drive electrodes, which are attached to the fixed support rim and span the entire width of the proof-mass. Anisotropic wet etching is performed at the end of the fabrication in order to release the proof-mass as well as to remove un-needed silicon around the outside perimeter of the sense/drive electrodes as illustrated. The detailed individual device structures are explained in [24], [25]. The size of the three-axis chip is $7 \times 9$ mm$^2$. All three devices have large proof-mass (~2 milli-gram), large sense area ($1 \sim 3$ mm$^2$), and small sensing gap (<1.5 μm), resulting in high sensitivity and sub-μg/√Hz mechanical noise floor. The design specifications of the three-axis accelerometer system are summarized in Table I. As shown, both in-plane and out-of-plane devices have high sensitivity and sub-μg/√Hz mechanical noise.

III. FABRICATION

The three-axis accelerometer utilizes a combined surface and bulk micromachining technology, which has been well characterized to build individual devices [23]. The fabrication process is shown in Fig. 3. It is a seven-mask double-sided process.

The process starts with a shallow 3.5-μm-deep p++ boron diffusion on both sides of a ⟨100⟩ double-side polished p-type silicon wafer, defining the thickness of suspension beams and the area of the proof-mass and supporting rim. Then, 70-μm deep trenches are made by using Deep Reactive Ion Etching (DRIE). The trenches are then refilled completely with a combination of low-pressure chemical-vapor deposition (LPCVD) silicon oxide (sacrificial layer), silicon nitride, and doped polysilicon. The polysilicon trench refilling is used to form vertical sense/drive electrodes and high aspect-ratio springs to support the proof-mass for in-plane devices. In addition, the polysilicon in the refilled trenches also forms vertical stiffeners for the out-of-plane device. After polysilicon deposition, annealing is followed to alleviate any compressive stress in the polysilicon [26].

Next, the polysilicon and nitride films are etched using RIE and another LPCVD silicon oxide (capping oxide) is deposited. The oxide is patterned to form contact openings to the bulk silicon for the subsequent anisotropic wet etch in Ethylene-Diamine Pyrocatechol (EDP). Then, contact metal is electroplated. To minimize the etch time in the anisotropic wet etching and help undercut the electrodes for in-plane devices by the etchant, some of the single-crystal silicon is etched by DRIE. After the DRIE, anisotropic wet etching is followed not only to release the proof-mass and the supporting rim but also to etch the unnecessary silicon around the sense/drive electrodes for in-plane devices. This step is important to achieve high sensitivity in-plane devices. Details are explained in [24]. Finally, the sacrificial oxide layer is removed by etching in hydrofluoric acid (HF).

Fig. 4 shows a fabricated three-axis single-chip accelerometer. Two in-plane (x- and y-axis) and one out-of-plane (z-axis) devices are mechanically connected by polysilicon connectors. These connectors provide electrical isolation between individual devices to ensure cross-talk free operation as well as photographically-defined alignment accuracy. The connectors are not essential for the three-axis accelerometer and the accelerometer could operate without them. The connectors are added to monitor individual single-axis devices for testing purpose as well as to enable die separation of individual devices.

IV. TEST RESULTS

A. Sensor System Performance

The capacitance changes from the accelerometer are read out by using a switched-capacitor front-end, which is known to be immune to input parasitic capacitance [27]. This enables hybrid assembly of the three-axis accelerometer with the readout circuitry. In order to estimate the overall noise of the accelerometer.
Fig. 2. Individual device structures. (a) Out-of-plane accelerometer [25], [31]; (b) in-plane accelerometer [24].

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>THREE-AXIS SINGLE-CHIP ACCELEROMETER DESIGN SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>In-Plane</td>
</tr>
<tr>
<td>Operating range [g]</td>
<td>±1</td>
</tr>
<tr>
<td>Bandwidth [Hz]</td>
<td>100</td>
</tr>
<tr>
<td>Mass [milli-gram]</td>
<td>2.65</td>
</tr>
<tr>
<td>Sensing gap [μm]</td>
<td>1.2</td>
</tr>
<tr>
<td>Sense capacitance [pF]</td>
<td>7.7</td>
</tr>
<tr>
<td>Spring constant [N/m]</td>
<td>25</td>
</tr>
<tr>
<td>Sensitivity [pF/g]</td>
<td>6.8</td>
</tr>
<tr>
<td>Mech. Noise [μg/√Hz]</td>
<td>0.7</td>
</tr>
</tbody>
</table>

In a three-axis accelerometer system, the readout circuit noise needs to be taken into account. In this paper, noise represents the overall system noise unless it is stated as mechanical or electronic noise. The electronic noise of the readout circuit was measured as \( \sim 790 \, \text{nV/√Hz} \) at 1 MHz [20]. Assuming 0.2 V/pF circuit sensitivity, the estimated Input Referred Noise Density (IRND) can be calculated as

\[
\text{IRND}[\text{g/√Hz}] = \sqrt{N_{\text{mechanical}}^2 + \left( \frac{N_{\text{electronic}}}{\text{SystemGain}} \right)^2}
\]

where \( N_{\text{mechanical}}[\text{g/√Hz}] \) is mechanical noise, \( N_{\text{electronic}}[\text{V/√Hz}] \) is electronic noise, and SystemGain [V/g] is the product of sensitivities of the accelerometer and readout circuit. From design specifications of the accelerometers, the estimated IRND of the out-of-plane and in-plane accelerometers with readout electronics is expected to be 1.53 μg/√Hz and 0.91 μg/√Hz, respectively.
Fig. 3. Fabrication process. (a) Boron doping; (b) DRIE trench; (c) oxide, nitride, poly deposition; (d) pattern oxide, nitride, poly; (e) electroplate metal; (f) anisotropic etching; (g) HF release.

B. Electrostatic Measurement

The three-axis chip has been tested electrostatically. Electrostatic measurement shows pull-in voltages of 1.9 and 2.5 V for in-plane, and 3.7 V for out-of-plane devices as shown in Fig. 5. This indicates spring constants of 17.1, 19.5, 12.0 N/m, for X, Y, Z axis accelerometers, respectively. Note that the out-of-plane device has higher pull-in voltage than the in-plane devices since we performed the electrostatic test on a flat stage where the out-of-plane device experiences the 1 g gravitational bias. In order to extrapolate the spring constant of the out-of-plane device from its pull-in voltage, we took this 1 g bias effect into account. The out-of-plane device has a lower spring constant than expected. It is because the boron doping level of the particular batch of wafers was lower than expected and resulted in a smaller thickness for the support beams, which gives a smaller spring constant. The spring constants of the in-plane devices are close to the estimated values.

C. Dividing Head (Precision Turn Table) Measurement

Fig. 6 shows measured differential capacitance vs. input acceleration by using a dividing head (i.e., precision turn table) and a HP-4284A precision LCR meter. Note that in-plane devices have smaller offset (0.09 pF) than the out-of-plane device (0.2 pF). The offset for the out-of-plane device (\( |\Delta C_{\text{Top}} - \Delta C_{\text{Bottom}}| \)) at zero acceleration) is due to gap variation on top and bottom of the wafer. However, the offset for in-plane devices (\( |\Delta C_{\text{Right}} - \Delta C_{\text{Left}}| \)) at zero acceleration) is more immune to fabrication variation. In the range of \( \pm 0.3 \) g, the three-axis chip provides sensitivity of 8.0, 7.9, 4.9 pF/g for X, Y, Z axes, respectively, with a small offset and good linearity. The measured sensitivities of in-plane and out-of-plane devices are \( \sim 15\% \) and 70\% higher than estimated, respectively. This is because fabricated accelerometers have lower spring constants and larger sensing gaps, very sensitive to the sensitivity (proportional to \( 1/d^3 \)), than expected.

D. Hybrid Module With Switched Capacitor Readout Circuit

Capacitance changes produced by the accelerometer are read out using a \( \Sigma - \Delta \) switched capacitor circuit, which can operate either in open- or closed-loop. The circuit includes chopper stabilization and correlated double sampling to cancel 1/f noise, amplifier offset and compensate for finite amplifier gain. It operates using a 1 MHz clock and can resolve better than 10 aF (\( \sim 10 \) Hz) with dynamic range of 120 dB for 1 Hz BW, while dissipating less than 12 mW from 5 V supply [27]. Fig. 7 shows a hybrid three-axis accelerometer with two CMOS \( \Sigma - \Delta \) readout circuits in a dual inline package (DIP). Each readout circuit contains two \( \Sigma - \Delta \) readout circuits and external reference capacitors are used to establish a full-bridge scheme. The size of the
Fig. 6. Measured capacitance change vs. input acceleration shows sensitivities of 8.0, 7.9, 4.9 pF/g for X, Y, Z axes.

Fig. 7. Hybrid accelerometer module in a DIP package.

The entire package is $3 \times 4.5 \times 1$ cm$^3$. The mounting of the device on a Printed Circuit Board (PCB) is critical for the three-axis accelerometer because the device has double sided features such that it needs to be suspended from the PCB. A nonconductive epoxy has been used to mount the device. The epoxy is cured at 100°C for 2 h after the device is mounted. Although this method is not an optimal approach to reduce sensitivity due to Coefficient of Thermal Expansion (CTE) mismatch, it is the best approach available due to its simplicity. An improved packaging and mounting scheme will be necessary to realize devices with improved temperature performance.

In-plane and out-of-plane accelerometers combined with readout circuit provide system gain of 0.49 and 0.96 V/g, respectively. We do not know the source of this discrepancy. The open-loop output noise of the hybrid module and a 50 kΩ reference resistor are measured with a HP 3561 dynamic signal analyzer, and shown in Fig. 8. This figure shows that the resistor has 32 nV/$\sqrt{\text{Hz}}$ noise density which matches well with estimated thermal noise of the resistor (note that the measurement bandwidth is 11.72 Hz in these measurements and $\sqrt{2}$ is included to account for the two output channels of the readout circuit). The hybrid module shows higher noise density for both in-plane and out-of-plane devices at low frequency. The in-plane device can resolve 13.8 $\mu$g-rms at 100 Hz and 5.5 $\mu$g-rms above 1.5 kHz, which correspond to IRND of 4.0 $\mu$g/$\sqrt{\text{Hz}}$ at 100 Hz and 1.60 $\mu$g/$\sqrt{\text{Hz}}$ above 1.5 kHz, respectively. On the other hand, the out-of-plane device shows 9.34 $\mu$g-rms at 100 Hz and 3.7 $\mu$g-rms above 600 Hz, which indicate IRND of 2.7 $\mu$g/$\sqrt{\text{Hz}}$ at 100 Hz and 1.08 $\mu$g/$\sqrt{\text{Hz}}$ above 600 Hz, respectively. Table II summarizes the measured specifications of the three-axis accelerometer, the interface circuit, and the hybrid module.

E. Temperature and Drift Characteristics

The drift of the accelerometer is determined primarily by the package and assembly. Therefore, to determine the true stability of the device, the packaging approach needs to be improved. As mentioned in the previous section, the packaging scheme of the current system is not optimum. Nevertheless, the temperature and drift characteristics of this system have been measured in an environmental chamber (ESPEC-SU240).
TABLE II
MEASURED THREE-AXIS ACCELEROMETER SYSTEM SPECIFICATIONS

<table>
<thead>
<tr>
<th>CMOS readout electronics</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity</td>
<td>0.2 V/pF</td>
</tr>
<tr>
<td>Electronic Noise</td>
<td>790 nV/√Hz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>3-axis single-chip accelerometer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity [pF/g]</td>
</tr>
<tr>
<td>----------------------------------</td>
</tr>
<tr>
<td>Mech. Noise [μg/√Hz]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MEMS device and interface circuit module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity [V/g]</td>
</tr>
<tr>
<td>Noise floor [μg/√Hz]</td>
</tr>
</tbody>
</table>

* denotes estimated.

Fig. 9. Temperature and drift characteristics show TCO of 500 ppm/°C up to 80 °C and drift of ~400 ppm for 1 h.

Fig. 9 shows rest capacitances that were recorded by using a LCR meter every 1 min for 1 h at 25 °C, 50 °C, and 80 °C. The temperature coefficient of offset (TCO) is obtained to be 70 ppm/°C up to 50 °C and 500 ppm/°C up to 80 °C ([C_{at 80 °C} - C_{at 25 °C}]/C_{at 25 °C}/ΔT). This is mainly caused by the CTE mismatch of the device and its packaging. CTE of the materials used for the device itself such as silicon, polysilicon, silicon nitride are 2.4–2.9 ppm/°C, while PCB and nonconductive epoxy have CTE of 20–25 ppm/°C and 40–60 ppm/°C, respectively [28]–[30]. This indicates that packaging and assembly techniques are major limiting factors. Thus, improved packaging and assembly techniques are expected to significantly reduce TCO. The drift of the accelerometer is also measured from room temperature up to 80 °C. The measurement data shows ~400 ppm for 1 h at 50 °C (Standard deviation of C_{at 50 °C}/C_{at 50 °C}).

V. CONCLUSION

A single-chip three-axis silicon capacitive accelerometer with a switched-capacitor front-end Σ–Δ modulator readout circuitry is demonstrated with micro-g resolution. The accelerometer is a monolithic integration of three individual single-axis accelerometers. Utilizing a combined surface and bulk micromachining technology, full-wafer thick proof-mass, large sense area, small sensing gap (<1.5 μm) have been achieved. The fabricated accelerometer chip is 7 × 9 mm² in size, has >~5 pF/g measured sensitivity and sub-μg/√Hz mechanical noise floor for all three axes. The total measured noise of the accelerometer hybrid assembled with CMOS interface circuit is 1.60 μg/√Hz (>1.5 kHz), 1.08 μg/√Hz (>600 Hz) for in-plane and out-of-plane devices, respectively. The accelerometer has TCO of 70 ppm/°C up to 50 °C and 500 ppm/°C up to 80 °C. Drift of the accelerometer is measured to be ~400 ppm for 1 h.

ACKNOWLEDGMENT

The authors thank Dr. N. Yazdi and Dr. A. Salian for their contributions to the above work, R. Gordenker and B. Casey for device bonding and testing stages, and the staff at WIMS, The University of Michigan.

REFERENCES


Khalil Najafi (S’84–M’86–SM’97–F’00) was born in 1958. He received the B.S., M.S., and the Ph.D. degree in 1980, 1981, and 1986, respectively, all in electrical engineering from the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor. From 1986 to 1988, he was employed as a Research Fellow, from 1988 to 1990, as an Assistant Research Scientist, from 1990 to 1993, as an Assistant Professor, from 1993 to 1998, as an Associate Professor, and since September 1998, as a Professor and the Director of the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan. His research interests include: micromachining technologies, solid-state micromachined sensors, actuators, and MEMS; analog integrated circuits; implantable biomedical microsystems; hermetic micropackaging; and low-power wireless sensing/actuating systems.

Dr. Najafi was awarded a National Science Foundation Young Investigator Award from 1992–1997, was the recipient of the Beatrice Winner Award for Editorial Excellence at the 1986 International Solid-State Circuits Conference, of the Paul Rappaport Award for coauthoring the Best Paper published in the IEEE TRANSACTIONS ON ELECTRON DEVICES, and of the Best Paper Award at ISSCC 1999. In 2001, he received the Faculty recognition Award, and in 1994 the University of Michigan’s “Henry Russel Award” for outstanding achievement and scholarship, and was selected as the “Professor of the Year” in 1993. In 1998, he was named the Arthur F. Thurnau Professor for outstanding contributions to teaching and research, and received the College of Engineering’s Research Excellence Award. He has been active in the field of solid-state sensors and actuators for more than eighteen years, and has been involved in several conferences and workshops dealing with solid-state sensors and actuators, including the International Conference on Solid-State Sensors and Actuators, the Hilton-Head Solid-State Sensors and Actuators Workshop, and the IEEE/ASME Micro Electromechanical Systems (MEMS) Conference. He is the Editor for Solid-State Sensors for IEEE TRANSACTIONS ON ELECTRON DEVICES, Associate Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS, an Associate Editor for the Journal of Micromechanics and Microengineering, Institute of Physics Publishing, and an editor for the Journal of Sensors and Materials.