Proposal to the Consortium for Embedded and Internetworking Technologies

Proposal Title: Hardware-Software Co-design of Network Processors and Packet Classification

Scope of the proposed Activity:

(i) Specification and Modeling
(ii) Composition, Synthesis and Optimization
(iii) Performance Analysis and Evaluation

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Abstract

Advances in modern CAD tools and design methodologies enable the design of complex electronic systems under short time-to-market constraints. In this research proposal, the term Network Processor system refers to non-homogeneous distributed real-time system composed of network processors and general purpose processors. Such a system may be implemented as a single chip, a board or a geographically distributed system. In a traditional design methodology, designers make the hardware/software partitioning at an early stage of the development cycle. The different parts of the system are designed by different groups. A specification, often incomplete and written in non-formal languages, is developed and given to the hardware and software engineers. Designers often strive to make everything fit in software and off-load only some parts of the design to hardware to meet timing constraints. Any design error is detected only at a late stage during system integration, often leading to a longer delay and a higher cost. In addition, the partition decision made at an early stage, restraints the ability of the designer to investigate a better trade-off. The different parts of the system are generally over-sized in order to reduce last-minute risks. We propose to develop a method (or a tool) to handle the design of mixed hardware/software Network Processor systems starting from system-level specification. The co-design or embedded system design tool is expected to provide a drastic increase in the productivity that may be used to explore several architectural solutions and to reduce the cost of the final design.

One of the main tasks of a network processor is *packet classification.* The techniques used for packet classification are extremely critical, since packet classification plays a significant role in determining the performance of the network processor in a high-speed environment. In this project, we propose to investigate the packet classification task in network processors. First, we propose to examine and compare the performance of the existing algorithms for the task under realistic network traffic conditions (e.g., non-Poisson traffic in practical multi-hop network settings). Such a study will provide an in-depth understanding of the interaction between various issues involved in packet classification and will help to identify the bottlenecks. This will lead to the development of new

techniques to overcome the bottlenecks. The novel techniques developed as a part of this project for packet classification will be evaluated through simulations and formal analysis.

The deliverables of this project will include simulation codes developed for the evaluation of the packet classification and for the hardware-software co-design framework.

If this project is funded, we see a potential for seeking for external matching funds for continued research in the topics above from government agencies, as for example from NSF. In particular, the funding of this project entitles Dr. Richa to apply for matching funds from NSF, as a provision of her NSF CAREER Award. Through the direct involvement of graduate students in the project and through the incorporation of the research results of this project into courses taught by the PIs at ASU, the project will have a significant positive impact on education and on the human resource base in the Phoenix metropolitan area.