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Automatic antenna-tuning unit for software-defined and cognitive radio

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Summary

This paper discusses the implementation of an automatic antenna tuning unit system (ATU) for software-defined and cognitive radio. The ATU simplifies radio frequency (RF) front-end design for multi-band, multi-mode radios by allowing an electrically small reconfigurable antenna to become a frequency-agile selective component (essentially a tunable filter). In implementing the ATU, impedance synthesizers (tunable matching networks) using RF MEMS switches as the control elements are used to match a more or less arbitrary load to a convenient impedance value. To generate feedback data that can be used to optimize the impedance synthesizer, the incident and reflected powers at the input to the impedance synthesizer are sampled using a power sensor block comprising directional coupler, logarithmic RF power detectors, analog-to-digital converters (ADCS), and return loss computation algorithms running on a field programmable gate array (FPGA). From a practical point of view, in order to be compatible with commercial wireless handset devices, we propose to design and ultimately implement a fully integrated ATU system. In this paper, a hard- ware implementation of the ATU prototype has been demonstrated to verify narrowband automatic tuning ability of the ATU under constantly changing environment conditions, and we present simulated results for a logarithmic power detector designed with 55 dB dynamic range over the 800 MHz–2 GHz frequency band using 0.25 μ CMOS technology. Copyright © 2007 John Wiley & Sons, Ltd.

KEY WORDS: antenna; software-defined radio; adaptive tuning

1. Introduction

At the present time, there is tremendous demand for antennas with high efficiencies in very small form factors that fit inside ever-shrinking portable wireless devices like handsets and personal digital assistants. These antennas must cover a variety of frequency bands and support different wireless standards. Traditionally, antenna engineers have designed antennas for these applications using computationally intensive full-wave electromagnetic simulation followed by long hours in the lab tweaking performance. It has become increasingly apparent that the requirements of software-defined radio (SDR) and its proposed successor, cognitive radio, will render this approach untenable. In References [1–5], a new approach for using electrically small radiating structures in multi-band, multi-mode radio transceivers is discussed. In this approach, the narrow instantaneous bandwidth of the radiator is automatically tuned over a much

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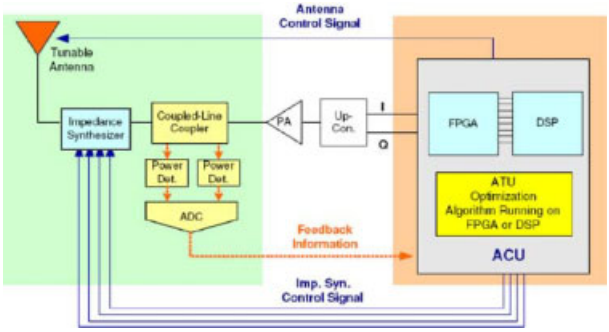

Fig. 1. Block diagram of closed-loop automatic antenna-tuning unit (ATU).

wider frequency range by an automatic antenna-tuning unit (ATU). Furthermore by exploiting the natural frequency selectivity of an electrically small antenna (ESA), radio frequency (RF) front-end design for multi-band, multi-mode radios is simplified by reducing the requirements for analog filters [1,2].

The basic block diagram of the ATU system is shown in Figure 1. A gross frequency step is enabled by changing the state of a control element in the antenna aperture. This open-loop tuning feature is supplemented by a closed-loop matching scheme that ensures that the narrowband antenna is automatically matched to any desired frequency under all environmental conditions with circuits using practical component values and tolerances. As the block diagram reveals, the antenna system is no longer simply an electromagnetic transducer, but a mixed-signal system that involves several microelectronics circuits as well as appropriate software algorithms running on one or more programmable logic devices (PLDs) such as field programmable gate arrays (FPGAs) or digital signal processors (DSPs). Implementation of the ATU includes the design and fabrication of an impedance synthesizer, coupled-line directional coupler, RF power detectors, analog-to-digital converters (ADCs), and an antenna control unit (ACU). In order to validate the design of the ATU, a hardware implementation of the ATU prototype has been demonstrated to verify narrowband automatic tuning ability of the ATU under constantly changing environment conditions. The proof of concept of the reconfigurable antenna technology has opened up several possibilities for future research. One important area is the IC implementation of the ATU. In this paper, we discuss some issues with on-chip realization of the ATU system, focusing especially on a CMOS RF power detector for the ATU.

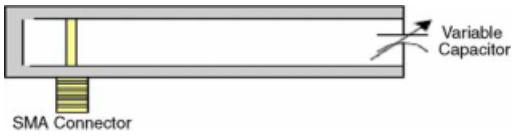

Fig. 2. Geometry of shorted patch antenna (SPA) for reconfigurable antenna implementation.

2. Automatic Antenna Tuning Unit

In this section, we discuss the major issues in ATU design. These include the design, fabrication, and measurement of the electrically tunable antenna, impedance synthesizer, RF power sensor, and analog and mixed-signal control circuitry.

2.1. Electrically Tunable Antenna

In principle, ESAs can be utilized as tunable filters as well as radiating elements resulting in a simplification of the radio's RF front-end design. This novel approach has the potential to lower the cost of next generation commercial and military radios while simultaneously enhancing performance [1–4]. In this work, an electronically tunable shorted patch antenna (SPA) was designed and fabricated in order to demonstrate the frequency selectivity of ESAs for the ATU system.

The geometry of the SPA is shown in Figure 2. The SPA is built with a layer of copper supported by FR4 over air as the main substrate. To feed the SPA, the outer conductor of the SMA connector is connected to the ground plane while the inner conductor is connected to the patch. The SPA is loaded with surface mount device (SMD) capacitors at the radiating edge to effectively change the electrical length of the antenna. Along with the capacitor, a PIN diode switch and its associated bias network are mounted on the underside of the ground plane. Figure 3 describes the tuning circuit used for the SPA. When the voltage on *CNTL* is low, the PIN diode switch is off, so $C = C1$. When *CNTL* is high, $C = C1 + C2$. With the increased capacitance at the radiating edge, the SPA is tuned to a lower frequency band.

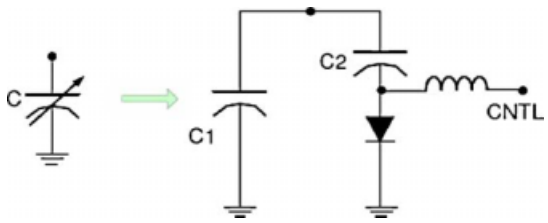

Fig. 3. Tuning circuit for the reconfigurable SPA.

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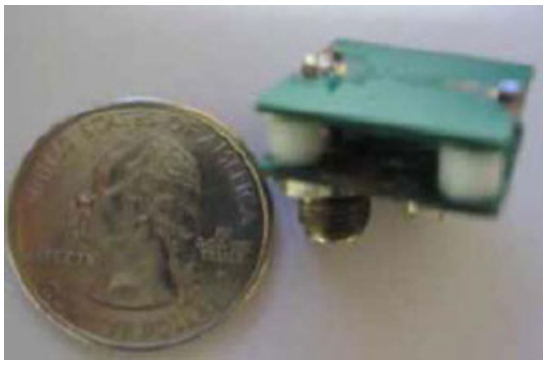

Fig. 4. Photo of the fabricated reconfigurable SPA.

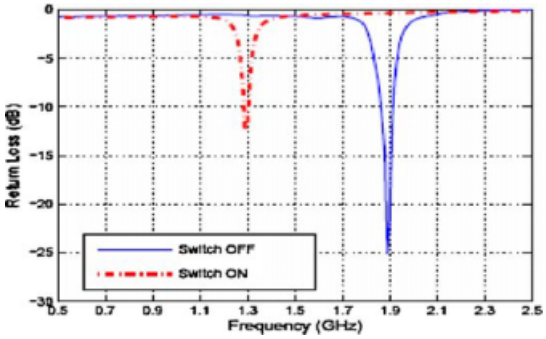

Fig. 5. Measurement results (S_{11}) of the reconfigurable SPA.

A photo of the fabricated SPA is shown in Figure 4. The measured return loss for each state is presented in Figure 5. It has been found that the response of the fabricated tunable antenna is very sensitive to its surrounding environment. In this paper, we overcome this issue by implementing an automatic ATU.

2.2. Impedance Synthesizer

To provide a complex-conjugate matching capability for a wide range of antenna impedances under changing environments, a lowpass-type pi-matching network is considered due to its harmonic rejection capability and wide matchable impedance range [5,6]. Figure 6 illustrates the basic topology of the impedance synthesizer. With a fixed inductor and two variable capacitors, the matching network is capable of generating a wide range of tuning possibilities. Although the matching network would provide better tunability if a variable inductor was used, we avoided the use of a tunable inductor to simplify the ATU design. The values of L, $C1_{\min}$, and $C2_{\min}$, and the numbers ($N1$ and $N2$) of capacitors in the configuration are determined by the desired operating frequency and required range of impedances to be matched (i.e., the matchable domain).

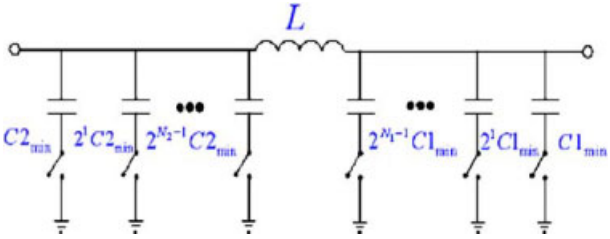

Fig. 6. Impedance synthesizer configuration.

A series of simulations has been performed by varying N_1, N_2, L, $C1_{\min}$, and $C2_{\min}$ in order to obtain reasonable matchable domains for the frequency range of 800–1900 MHz. Figure 7 shows the matchable domains at different frequencies. Each dot on the Smith Charts represents an antenna impedance that can be matched exactly to the system impedance of 50 Ω.

It is important to note that this matching network topology is capable of producing a perfect match as long as its component values are variable from zero to infinity. However, the practical component values that can be realized are limited. The practical realization of the impedance synthesizer involves complicated trade-offs between the matching domain and physical limitations of components [7]. The losses and parasitic effects associated with the switch elements are one of the most important considerations when implementing the impedance synthesizer because they can deteriorate its performance drastically.

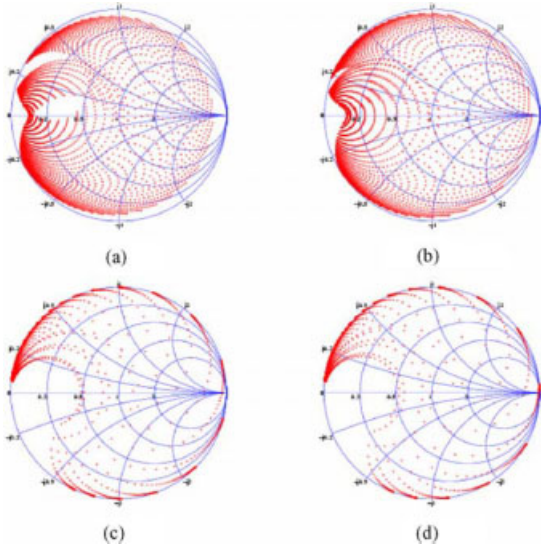

Fig. 7. Simulated matchable domain with 12 capacitors ($N_1 = N_2 = 6$, $2^{12} = 4096$ states) at (a) 800 MHz, (b) 900 MHz, (c) 1800 MHz, and (d) 1900 MHz. Ideal components are used in the simulation for the pi-network of Figure 6 with $L = 3$ nH, $C1_{\min} = 0.5$ pF, and $C2_{\min} = 1$ pF.

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In general, variations of antenna impedance due to the environmental conditions are limited to a certain region of the Smith Chart. Thus, it is not necessary for the dynamic range of an impedance synthesizer to cover all the Smith Chart area, but be sufficient to generate the complex conjugates of the antenna impedances confined to a certain region on the Smith Chart. In other words, fabricating an impedance synthesizer for the purpose of matching a *particular* antenna (as opposed to *any* antenna) will require only a small tuning range of capacitors. Therefore, careful engineering trade-off analyses are necessary to determine the optimal number of matching states with an acceptable dynamic range.

Since the impedance synthesizer uses switching elements, the loss and parasitics inherent in RF switches can reduce the overall system efficiency. Moreover, for high power application the nonlinearity of the switches can generate spurious frequency radiation and distortion of the signal. In order to provide acceptable performance of the impedance synthesizer in the frequency range of 800 MHz–2 GHz, the use of RF MEMS switches in the impedance synthesizer is probably imperative. RF MEMS switch is attractive for the impedance synthesizer because it shows low-loss, low-parasitic, and high linearity over wide band [8].

The impedance synthesizer should be able to reconfigure its characteristics fast enough to compensate the constantly varying conditions in an antenna's environment. Moreover, to be compatible with the wireless protocol standards such as frequency hopping techniques, the duration of the tuning process should be short enough to constantly provide an optimum matching condition. The two crucial parameters of the system required to realize a high-speed ATU are switching time of the RF switches comprising the impedance synthesizer and sampling time of both ADC and ACU.

For demonstration purposes an impedance synthesizer with four RF MEMS switches ($2^4 = 16$ states) was fabricated. Figure 8 shows the photo of the fabricated impedance synthesizer with the TeraVicta's RF MEMS (TT712-68CSP) switches having hot switching capability (switch speed < 100 μS, typical hot switch life cycle = 1 *M*). Notice that from the figure the on/off status of the each capacitor is realized by shorting one output port of the switch while the other port is left open. The *S*-parameters of the fabricated impedance synthesizer were measured, and Figure 9 shows the measured matchable domain of the impedance synthesizer. The measurements agree well with simulations.

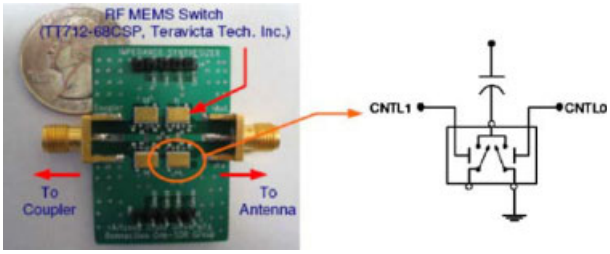

Fig. 8. Photo of the fabricated impedance synthesizer with RF MEMS switches.

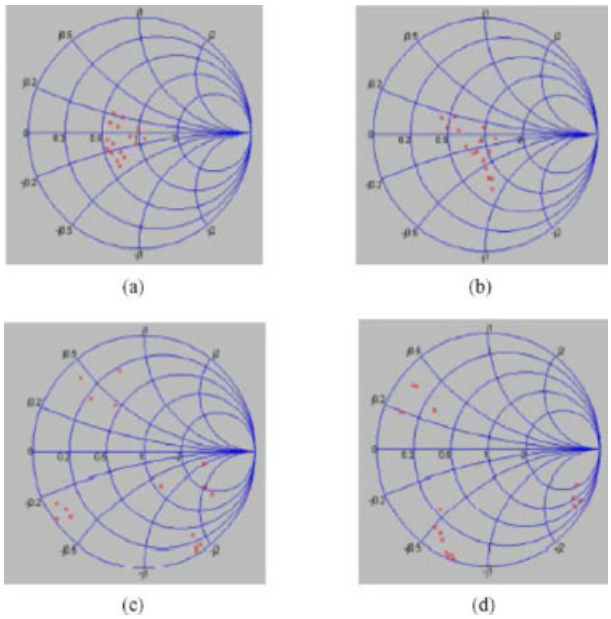

Fig. 9. Measured matchable domain of the fabricated impedance synthesizer with four capacitors at (a) 800 MHz, (b) 1000 MHz, (c) 1800 MHz, and (d) 1900 MHz.

2.3. RF Power Sensor

To provide the feedback information (i.e., incident and reflected power level between the antenna and impedance synthesizer) required to find an optimum matching status of the impedance synthesizer, an RF power sensor block consisting of a coupled-line directional coupler, RF power detectors, and ADCs is discussed here. In certain applications (e.g., CDMA), the incident power level is constantly being adjusted to optimize signal-to-interference-plus-noise ratio for all users. Hence, it is generally necessary to measure incident power levels as well as reflected power levels in order to accurately determine the input reflection coefficient.

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2.3.1. Directional coupler

The main design issue of the directional coupler is to sense the incident and reflected powers (with a reasonable power level required for an RF power detector), while delivering the input power to the antenna with minimum loss. For the concomitant weak couplings, a coupled-line coupler is appropriate for our ATU system. The directional coupler was designed with the help of Ansoft HFSS and fabricated on FR4 board (for more detail, see Reference [7]).

2.3.2. RF power detector

An RF power detector is used to convert the signals extracted from the coupled-line coupler to analog output voltage levels representing signal power. These voltages are then used as an input to an ADC. The LTC5534 logarithmic-based RF power detector (Linear Technology Corp.) is chosen here to detect the coupled power levels because of its large dynamic range. The RF power level in decibel scale at the input of the power detector is converted into DC voltage on a linear scale. To reduce overall system size, the coupled-line coupler and RF power detector are combined on a single PCB as shown in Figure 10.

In order to evaluate the performance of the power detector when it is connected to the coupled-line coupler, system level simulations were performed based on the measured responses of the coupler and power detector. Figure 11 shows the voltage outputs of the power detectors plotted as a function of antenna reflection coefficient, Γ_{ant}, at different input power levels available at the input port of the coupler. It is interesting to note that the voltage output at the reflected coupled port (i.e., V_{ref}) is converging when the reflection coefficient Γ_{ant} is very small. That is because, when the Γ_{ant} is very small, the power available at the reflected coupled port is mainly due to the power

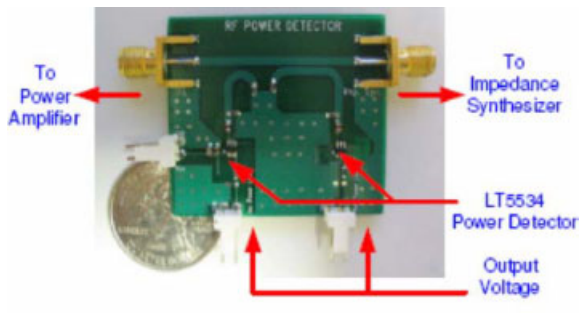

Fig. 10. Photo of the power detector combined with the three-line directional coupler.

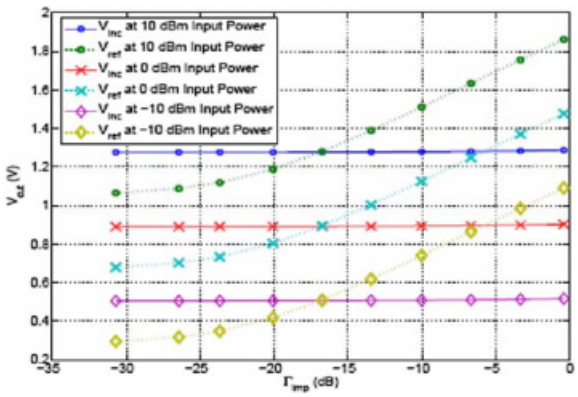

Fig. 11. V_{out} versus Γ_{ant} with different input power levels at 900 MHz.

coupled from the incident port, which is due to the finite isolation between the input and reflected coupled ports. Figure 12 shows that difference of V_{ref} and V_{inc} is not a function of the input power level, which makes the power-detection scheme robust with dynamic input power variations.

2.3.3. Analog- to-digital converter (ADC)

After detecting the incident and reflected power level with the RF power detectors, it is necessary to convert the analog signal to a digital signal for use in the ACU. In order to monitor the real-time performance of the power sensor, the National Instruments USB-6009 data acquisition board in conjunction with LabVIEW software is utilized. The LabVIEW program running on a PC digitizes the analog voltage levels and then sends the digitized information to the ACU via digital I/O lines of the board.

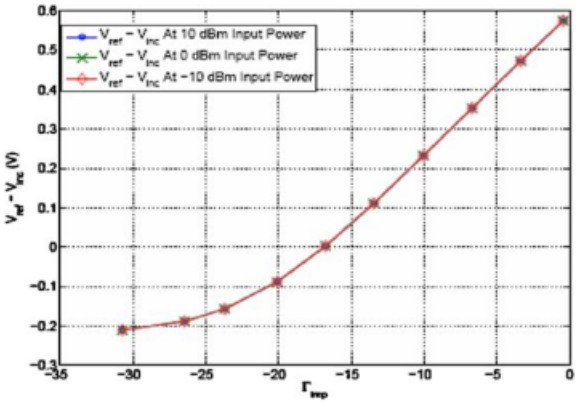

Fig. 12. $V_{ref}-V_{inc}$ versus Γ_{ant} with different input power levels at 900 MHz.

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2.4. Antenna-Control Unit (ACU)

The role of the ACU is to reconfigure the antenna and impedance synthesizer such that the matching state is optimum by generating the required switch control signals. After the antenna is reconfigured by the open-loop ACU based on the operating frequency information, the ATU closed-loop system operates to ensure that the coarsely tuned antenna is automatically matched to any given frequency under all environmental conditions. Based on the coupled incident and reflected signal levels, a search algorithm running on the ACU tries to minimize the impedance mismatch of the antenna. In this work, we used a simple nearest neighbor search algorithm [5,7].

The search process starts from an arbitrary point on the two-dimensional plane. The algorithm compares the ratios of the incident and reflected power levels detected at the starting point and its four nearest neighboring states. From among these five points, the one that generates a minimum ratio of these power levels is selected as the new starting point. The search continues to iterate until it finds a starting point that produces a smaller mismatch than any of its nearest neighbors.

The tunable antenna and impedance synthesizer control algorithms are programmed using very high-speed integrated circuit hardware description language (VHDL) and implemented using a FPGA device (Altera UP2 Education Board, Altera Corp.).

3. ATU Prototype and Test

In order to experimentally verify the ATU functionality, the overall ATU prototype system was assembled and tested as shown in Figure 13. The RF MEMS switch-based impedance synthesizer of Figure 8 was placed next to the electronically tunable antenna. The power detector combined with the coupled-line coupler was inserted between the impedance synthesizer and an RF MEMS switch (MagLatch^{TM} RF Switch, Magfusion, Inc.). This RF MEMS switch is not a part of the ATU, but employed to automatically switch between an RF signal generator (Agilent E4432B Signal Generator) and vector network analyzer (HP-8510C Vector Network Analyzer). In order to monitor the real-time performance of the ATU, the National Instruments USB-6009 data acquisition board is used in conjunction with LabVIEW software. LabVIEW routines were written to display the incident and reflected power levels, the difference between the detected power levels, and the status of the control switches within the impedance synthesizer. The network analyzer is connected to the PC by a GPIB, and the LabVIEW software also displays the return loss of the ATU system on the PC screen.

First, consider the case where the frequency of an RF signal applied to the input of the directional coupler (output of the signal generator) is set to 1.87 GHz. Initially, the state of the control element in the aperture of the SPA is set by the open-loop ACU [7,9]. The solid line of Figure 14 is the measured return loss of the SPA in this state. Next, the closed-loop scheme using a nearest neighbor search algorithm running on the FPGA tries to minimize the impedance mismatch between the antenna and impedance synthesizer. The dotted line of Figure 14 shows the results achieved by the ATU prototype. As can be seen in the figure, the ATU enables the highly selective frequency response of the SPA to be centered on the desired frequency.

Handheld devices are generally used under constantly changing environment conditions. To

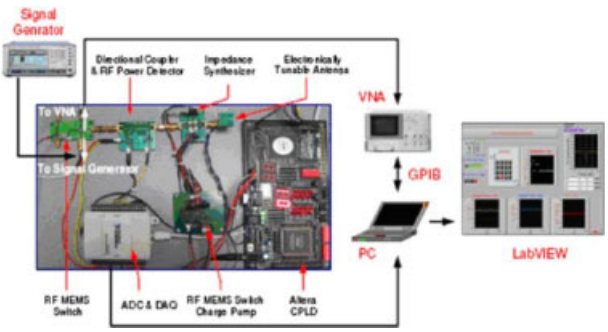

Fig. 13. Photo of the ATU and block diagram of the ATU demonstration setup.

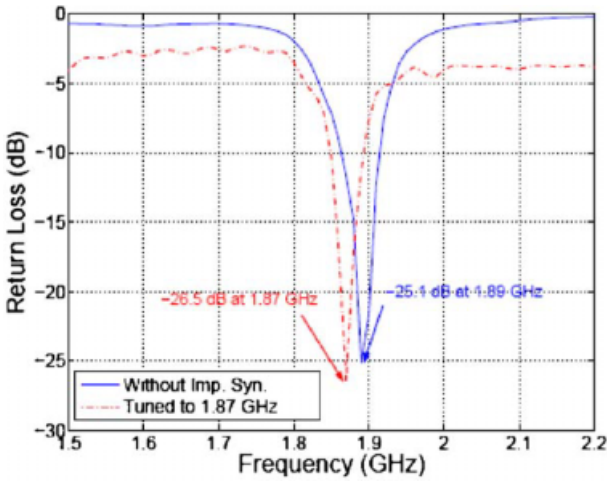

Fig. 14. Tuning ability of the ATU. The SPA is tuned to 1870 MHz.

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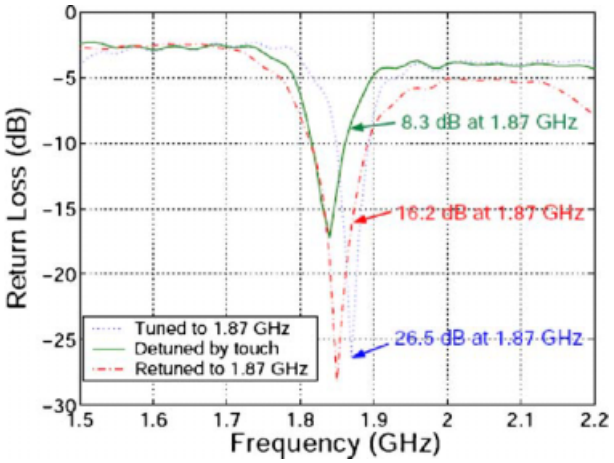

Fig. 15. Automatic tuning ability of the ATU.

demonstrate how well the ATU compensates for changing environmental conditions, the antenna is brought to close proximity of a human hand. Figure 15 shows the detuned response of the antenna when it is in contact with the hand. As can be seen, significant degradation of the antenna's performance occurs. Once the antenna is detuned, the search algorithm automatically reconfigures the impedance synthesizer to correct for this sudden environmental change. The retuned response, with the antenna still in contact with the hand, is shown in the same figure.

Many wireless devices need to support multi-band operation. To emulate this situation, the operating frequency is changed to 880 MHz. Based on the frequency information, the open-loop ACU first reconfigures the SPA to work at the lower frequency band as shown in Figure 16. Then the search algorithm finds an optimum switching configuration for the impedance synthesizer. The measured response after tuning is shown in the same figure.

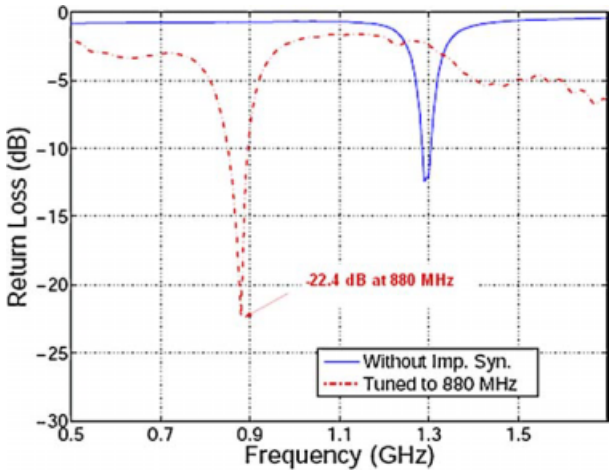

Fig. 16. Narrowband tuning ability of the ATU. The SPA is tuned to 880 MHz.

Designing a low-loss ATU is very important to maximize power transfer and minimize the noise figure (if used for a receiver system). However, the tunability and matching ability of the impedance synthesizer and the overall system efficiency of the ATU are mainly limited by the losses induced from RF switches, inductors, and capacitors. The degraded efficiency of the current prototype can be seen in Figures 14–16. The most promising technology for implementing low-loss switches, inductors, and capacitors is considered to be MEMS. MEMS technology offers high Q, low insertion loss, low-parasitic, and highly linear RF components.

4. IC Implementaion of the RF Power Detector

In order to increase the speed, lower the cost, and reduce the size of the circuits, it is desirable to ultimately fully integrate the entire ATU system onto a silicon chip using CMOS. The strategy we are using to implement the integrated ATU system is to develop the integrated parts one by one to replace their discrete equivalent in our prototype. The first part that we have designed and extensively simulated is the power detector which will be discussed here.

4.1. RF Power Detector Design

In order to cover a wide dynamic range (−40 dBm to +15 dBm) and operating frequency band from 800 MHz to 2 GHz, the power detector is realized using a logarithmic amplifier, and a piece-wise linear approximation is adopted for realizing the amplifier. The core of the logarithmic amplifier is a cascaded chain of several identical limiting amplifiers in combination with corresponding full-wave rectifiers and a low-pass filter as shown in Figure 17.

Since the log amplifier is based on piecewise-linear approximation, its accuracy is mainly determined by

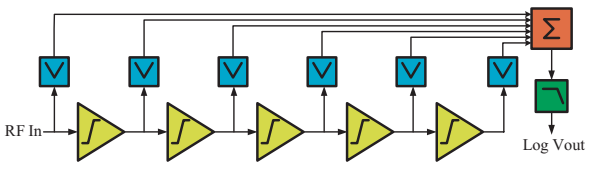

Fig. 17. Block diagram of logarithmic power detector.

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the number of stages of limiting amplifiers. The maximum deviation from an ideal logarithmic curve can be written as in Reference [10]

$$E_{\max}(\text{dB}) = \frac{10[(-1+\sqrt{A_S}+A_S)\log A_S-(A_S-1)\log(A_S^{(3A_S-1)/(2A_S-2)})]}{A_S-1} \quad (1)$$

where A_s is the linear gain of a single stage of the limiting amplifier, which is given by

$$A_S = \sqrt[N]{A_{\text{total}}} \quad (2)$$

where N is the stage number of the limiting amplifier, A_{total} is the overall gain of all N stages of limiting amplifier, which is equal to the input dynamic range, 55 dB or 526.34 V/V. This is because, in piecewise-linear approximation approach, small input is initially amplified linearly by N stages of limiting amplifiers with a total linear gain of A_S^N until it reaches a certain level at which it is clipped by the last stage of the limiting amplifier, and the gain becomes A_S^{N-1}. Henceforward, every time when input increases by a factor of A_S, the gain reduces A_S times. Thus an input with dynamic range of A_S^N corresponds N stages of limiting amplifier, where each stage has a linear gain of A_S.

Assuming a total gain of 55 dB, the number of gain stages versus maximum error is plotted in Figure 18. Requiring the measurement accuracy of the logarithmic amplifier to be 1 dB, we find that five limiting amplifier stages are needed. Given the overall gain of 55 dB and a bandwidth of 2 GHz for the five-stage limiting amplifier, the required gain and bandwidth of each stage are found to be 11 dB and 5.19 GHz, respectively,

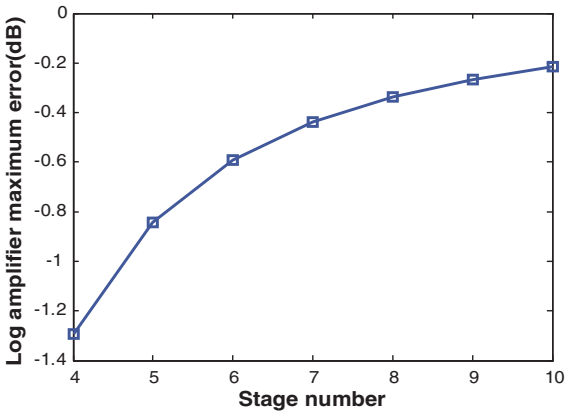
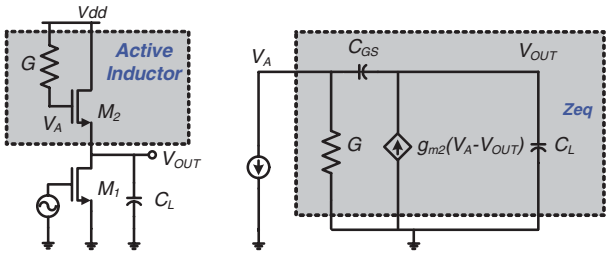


Fig. 18. Log amplifier error.



(a) (b)

Fig. 19. Active inductor shunt peaking. (a) Schematic (b) Small signal equivalent circuit.

where we assume that each limiting amplifier is a first-order stage to get a pessimistic estimation of the required bandwidth.

The required gain-bandwidth product (GBWP) of each limiting amplifier is thus about 18 GHz, which imposes a challenge to standard CMOS realization of the limiting amplifier. Therefore, certain bandwidth enhancement techniques must be used to both extend bandwidth and reduce the power consumption.

4.2. Active Inductor Shunt Peaking (AISP)

Inductor shunt peaking is commonly used to extended the bandwidth of an amplifier. However, because on-chip inductors take so much silicon area, they are often replaced by active inductors [11]. Figure 19 (a) shows the schematic of a common source (CS) amplifier with an active inductor load consisting of an NMOS and a resistor (conductance G). Its simplified small signal model is drawn in Figure 19 (b), where the effects of C_{GD} are neglected since the top NMOS device is in saturation region. Assuming M1 is ideal, the output impedance of the circuit is given as

$$Z_{\text{eq}}(s) = \frac{sC+G}{s^2CC_L+sG(C_L+C)+g_mG} \quad (3)$$

where $C = C_{GS} \approx 2/3C_{\text{gate}}$.

The effect of bandwidth extension by the active inductor shunt peaking can be observed by examining the difference in -3 dB frequencies between a regular NMOS load with resistor shorted in Figure 19 (a) and an active inductor load as the circuit intact in Figure 19 (a). In both load types, the DC gain is $1/g_m$. In the case of NMOS load, the -3 dB frequency is $\omega_1 = g_m/(C+C_L)$. Normalizing the magnitude of Equation (3) to $1/g_m$, frequency to ω_1, the frequency response of Z_{eq} is plotted in Figure 20, where we assume $C_L = 5C$.

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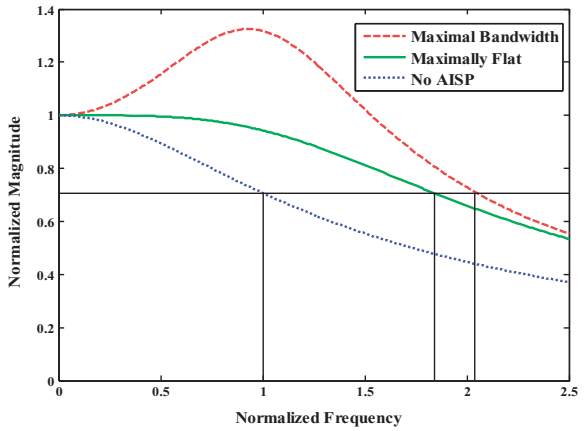

Fig. 20. Normalized frequency response of active inductor shunt-peaking.

In Figure 20, bandwidth can be maximally extended by a factor of 2.04 (dashed line) when $G = 0.36g_{\mathrm{m}}$. However, it causes a magnitude peaking of 32%. Since this is not desired, a flat frequency response is found when $G = 0.18g_{\mathrm{m}}$, in which case, the bandwidth (solid line) is 1.84 times of that of a regular NMOS load. For the purpose of comparison, the frequency response of a regular NMOS load is also plotted in the dotted line in Figure 20.

4.3. Active Negative Feedback (ANFB)

The block diagram of an ANFB circuit [12] is drawn in Figure 21. The basic idea is that in the feed-forward path, R_{L2}, C_2, and the transconductance cell G_{m2} act as a low-pass filter, so that the magnitude of the output rolls off as frequency increases. To offset this low-pass effect, active negative feedback is performed by a transconductance cell, G_{mf} to return a fraction of the output to the input of G_{m2}, so that the frequency roll-off can be cancelled out partially.

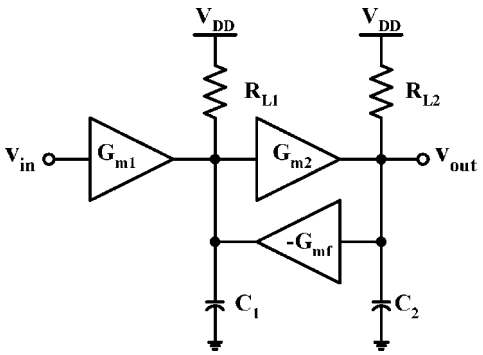

Fig. 21. Block diagram of an active negative feedback circuit.

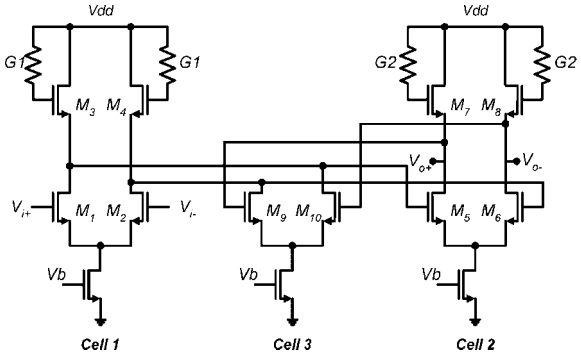

Fig. 22. CMOS limiting amplifier stage.

For a maximally-flat Butterworth response, the overall GBWP of the circuit in Figure 21 can be derived to be

$$A_{\mathrm{vo}} f_{-3\,\mathrm{dB}} \approx f_{\mathrm{T}} \frac{f_{\mathrm{T}}}{f_{-3\,\mathrm{dB}}} \tag{4}$$

where f_{T} is the cutoff frequency of the technology, A_{v0} and $f_{-3\,\mathrm{dB}}$ is the low frequency gain and the -3-dB frequency of the circuit, respectively. Since $f_{\mathrm{T}}/f_{-3\,\mathrm{dB}}$ is a factor larger than 1, Equation (4) indicates that active negative feedback can extend the overall GBWP beyond the technology cut-off frequency, f_{T}.

4.4. Limiting Amplifier

The schematic of a wideband limiting amplifier using both AISP and ANFB designed in TSMC 0.25 μm CMOS technology is illustrated in Figure 22. The frequency response of the limiting amplifier is simulated under the following four conditions: (1) all resistors shorted ($G1 = G2 = \infty$) and the feedback stage (cell 3) disconnected; (2) only feedback stage disconnected; (3) only all resistors shorted ($G1 = G2 = \infty$); (4) exact circuit of Figure 22. The gain bandwidth performance in each of the four cases is summarized in Table I. Normalizing the GBWP of the last three cases to that of the first case, we can draw the conclusion that by combining AISP and ANFB, the GBWP of the circuit can be extended by a factor of 1.9 without causing noticeable magnitude peaking.

Table I. GBWP improvement with AISP and ANFB.

Condition	Gain (V/V)	BW (GHz)	GBW (GHz)	GBW improvement
Without AISP, without ANFB	4.54	1.84	8.35	1
With AISP, without ANFB	4.54	3.20	14.53	1.74
Without AISP, with ANFB	3.75	2.87	10.76	1.29
With both AISP and ANFB	3.75	4.23	15.86	1.90

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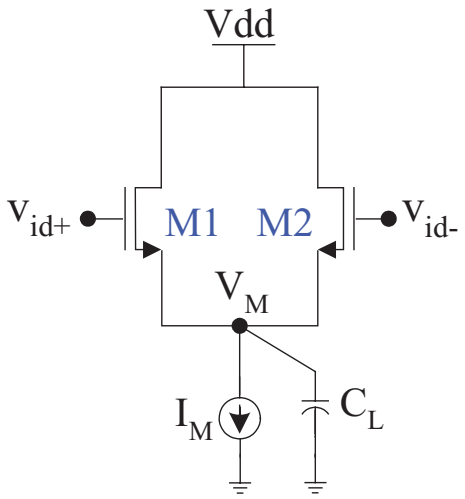

Fig. 23. CMOS rectifier and magnitude detector.

4.5. CMOS Rectifier and Magnitude Detector

Figure 23 shows the circuit diagram of the CMOS rectifier and magnitude detector [13]. With $M1$ and $M2$ biased in their weak inversion region, an AC signal is fed into the input pair; $M1$ and $M2$ switch on and off alternatively, and so act as a full-wave rectifier. C_L and output impedance at the source of $M1$ and $M2$ form a low-pass filter to remove the ripple of the rectified signal. The filtered DC voltage, V_{M}, with respect to the input magnitude, $|V_{\mathrm{IN}}|$, is given by

$$V_{\mathrm{M}} = \frac{1}{2}|V_{\mathrm{IN}}| + \left(V_{\mathrm{IN,cm}} - V_{\mathrm{TH}} - \sqrt{\frac{I_M}{K}}\right), \quad \text{for } |V_{\mathrm{IN}}| \geq \sqrt{\frac{I_{\mathrm{M}}}{K}} \qquad (5)$$

where $K = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{OX}}(W/L)_{M1,M2}$. Equation 5 shows that the output voltage V_{M} at the source of $M1$ and $M2$ is half of the input magnitude plus a fixed DC voltage, which is the second term in the parentheses.

4.6. Simulation Results of the Log Amplifier Power Detector

Figure 24 plots the frequency response of the five stages of the limiting amplifier, indicating a -3 dB bandwidth of 2.4 GHz, and overall differential gain of 56.9 dB. Figure 25 describes the input/output transfer curve of the log amplifier power detector at 900 MHz and 1900 MHz. The conversion gain at these two frequencies are 9.15 mv/dB and 8.46 mv/dB, respectively. Table II summarizes the simulated performances of the proposed logarithmic power detector.

Table II. Simulation results of the RF power detector.

Specifications	Required	Achieved by simulation
Dynamic range	-40 dBm$\sim$15 dBm	-50 dBm$\sim$15 dBm
Bandwidth	800 MHz$\sim$ 2 GHz	4 MHz$\sim$2.4 GHz
Gain	55 dB	56.9 dB
Power consumption	TBD	11 mA $\times$ 2.5 v $=$ 27.5 mW

5. Conclusion

In this paper, an ATU system has been presented for the further development of software defined and cognitive radio. The ATU provides a flexible antenna tuning capability using reconfigurable antenna technology and a closed-loop antenna tuning system.

One of the benefits of the ATU system is that it does not require *a priori* knowledge of antenna impedance which often varies dramatically in a constantly

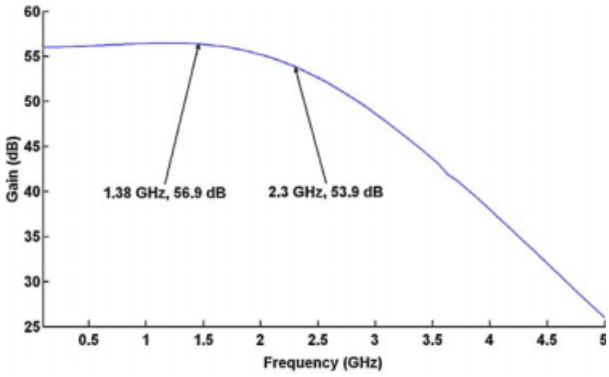

Fig. 24. Overall frequency response of the log amplifier.

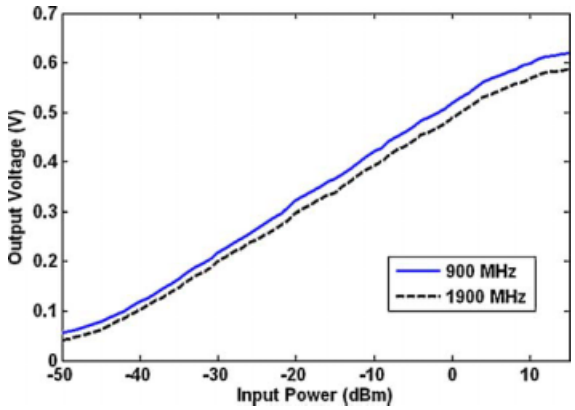

Fig. 25. Overall output voltage versus input power.

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changing environment. Additionally, its performance does not depend on precise control of matching network component values. Moreover, the ATU system will be able to automatically match almost any kind of antenna. By automatically reducing the mismatches at the output of a power amplifier module, the system can eliminate the need for an isolator which is an expensive and bulky component. We anticipate that such an ATU will be upgradeable to cover new frequency bands by simply upgrading its software, thus making it fully compatible with the goals of SDR and cognitive radio.

In the first step toward realizing a fully integrated ATU system, a logarithmic RF power detector using two bandwidth enhancement techniques was designed and simulated. By combining active inductor shunt-peaking and active negative feedback, the bandwidth of the limiting amplifier cell can be extended by a factor of 1.9 with almost no extra power consumption. To the best of our knowledge, this is the first time these concepts have been applied to a power detector circuit.

6. Considerations and Future Work

With the successful demonstration of the ATU prototype, it is expected that the ATU could be beneficial to future commercial and military SDR platforms. However, there are several issues to be considered for the ATU system to be deployed for use with these products. In order to meet the needs of the fast developing wireless and mobile services, further design and optimization of the ATU antenna system may be required to ensure high efficiency (low loss), low-power consumption, low profile, high-speed tuning, and spurious free radiation in a particular

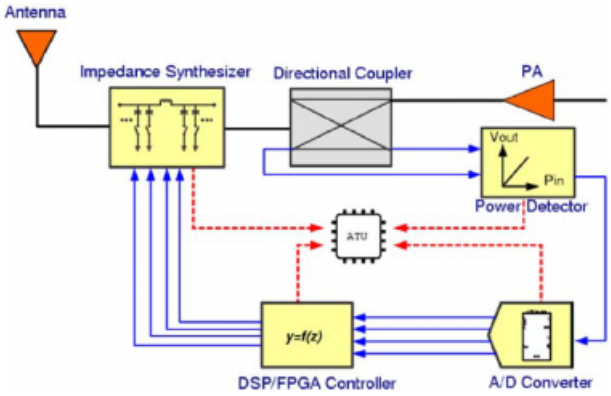

Fig. 26. IC implementation of ATU.

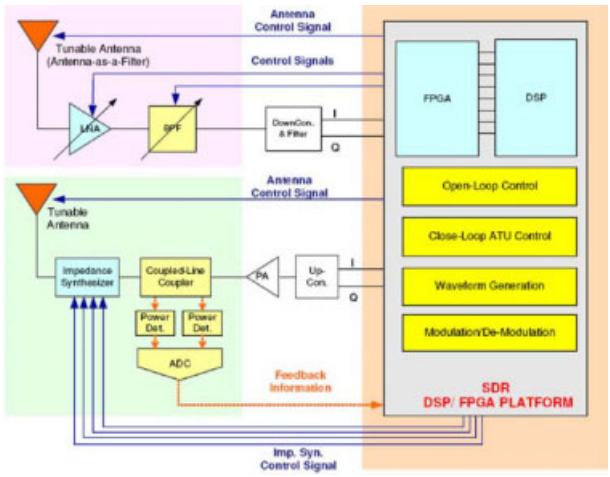

Fig. 27. Block diagram of a cognitive radio.

application.

The proof of concept of the reconfigurable antenna technology for SDRs has opened up several possibilities for future research. One important area is the IC implementation of the ATU. From a practical point of view, in order to be compatible with commercial wireless handset devices, we propose to design and ultimately implement a fully integrated ATU system as shown in Figure 26. Another area involves the use of a baseband SDR development platform to investigate efficient RF hardware reconfigurability. The prominent feature of the ATU is an automatic feedback tuning system with a digital control circuitry to maintain an optimum antenna matching condition. One of the most important considerations of the tuning system is to develop a software configuration which can control the RF hardware more efficiently. In order to develop and evaluate a variety of digital control schemes and algorithms, we propose to develop a software defined and cognitive radio prototype as shown in Figure 27. As can be seen in the figure, the radio system is based on a reconfigurable RF front-end and a digital signal processor (DSP)/FPGA hardware platform. Such reprogrammable radio system provides a rapid prototyping environment for the designs of a reconfigurable RF front-end testbed platform [14,15]. This study will also help to define the hand-held SDR terminals [16,17] and evaluate how the reconfigurable RF front-end can contribute to further developments of SDR.

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Sung-Hoon Oh received the B.S. degree from the University of Tennessee, Knoxville, in 2000, the M.S. degree from The Ohio State University, Columbus, in 2002, and the Ph.D. degree from Arizona State University, in 2006.

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During the Summer of 1993, Dr. Aberle was a NASA/ASEE Summer Faculty Fellow at NASA Langley Research Center. During the 1997/1998 academic year, Dr. Aberle took a sabbatical leave from Arizona State University. During his sabbatical, he was a Visiting Academic at the Royal Melbourne Institute of Technology in Melbourne, Victoria, Australia as well as a Visiting Researcher at Atlantic Aerospace Electronics Corp. in Greenbelt, Maryland.

Dr. Aberle recently returned to ASU after a 2-year leave-of-absence. During this leave, Dr. Aberle worked for a start-up company that provided innovative technological solutions for the wireless market.

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Chaitali Chakrabarti received her B.Tech. in Electronics and Electrical Communication Engineering from the Indian Institute of Technology, Kharagpur, India, in 1984. She received her Ph.D. from the University of Maryland, College Park, U.S.A., in 1990. She has been at Arizona State University since 1990 where she is now a Professor. Chaitali Chakrabarti's research interests are in the areas of VLSI architectures for signal processing, wireless communications and image processing, algorithm-architecture co-design of signal processing systems, low power embedded system design including joint energy and thermal management, memory design and compilation, system level optimizations for fuel cell powered systems, and CAD tools for VLSI. She has co-authored over 100 conference and journal articles in these areas. Her research is funded by the National Science Foundation and DARPA. Chaitali Chakrabarti is the Chair of the Technical Committee on Design and Implementation of Signal Processing Systems, IEEE Signal Processing Society. She has served on the program committees of ICASSP 1999, ISCAS 2002, SiPS 1995-2006, ISLPED 2001-2006, DAC 2002-2004, ASAP 2005-2006, HPCA 2006. She is the recipient of the 1994 Young Faculty Teaching Excellence Award and the 2001 IEEE Phoenix Chapter's Outstanding Educator Award.

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